

#### ■ Features

- World's thinnest, 0.25 mm (typical) height
- World's lowest power programmable oscillator, <3.5 mA typical current consumption
- 1-80 MHz frequency range. Contact SiTime for frequencies between 80 MHz - 110 MHz
- Extremely fast start-up time, <3 ms enabling power-cycling for lower system power
- Programmable standby or output enable modes
- <10  $\mu$ A current consumption in standby mode
- All-silicon device with outstanding reliability of 2 FIT, 10x improvement over quartz-based devices, improves system MTBF
- Outstanding mechanical robustness for portable applications
- Ultra short lead time
- Ideal for portable applications: High Capacity (HC) SIM cards, Smart cards, Near Field Communications (NFC), SD cards, multi-chip modules (MCM) and System-in-Package (SiP)

#### ■ Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	Contact SiTime for frequencies between 80 MHz - 110 MHz
Frequency Tolerance	F_tol	-100	–	+100	PPM	Inclusive of: Initial tolerance, operating temperature, rated power supply voltage change, load change, aging (1st yr@25°C), shock and vibration.
Storage Temperature Range		-55	–	+125	°C	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd		3.0	3.5	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
			3.5	4	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
Standby Current	I_std	–	3	10	$\mu$ A	Output is Weakly Pulled Down, $\overline{ST}$ = GND, Vdd = 1.8 V
		–	7	10	$\mu$ A	Output is Weakly Pulled Down, $\overline{ST}$ = GND, Vdd = 2.5 V, 2.8 V or 3.3 V
Duty Cycle	DC	45	–	55	%	All Vdds. f < 70 MHz
		40	–	60	%	All Vdds. f > 70 MHz
Rise/Fall Time	Tr, Tf	–	1.0	2	ns	20% - 80% Vdd level
Output Voltage High	VOH	90	–	–	%Vdd	IOH = -4 mA (Vdd = 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Voltage Low	VOL	–	–	10	%Vdd	IOH = 4 mA (Vdd = 3.3 V) IOH = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = 2 mA (Vdd = 1.8 V)
Input Voltage High	VIH	70	–	–	%Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30	%Vdd	Pin 1, OE or $\overline{ST}$
Input Current	I_in	–	–	10	$\mu$ A	
Output Load	Ld	–	–	15	pF	Maximum frequency and supply voltage. Contact SiTime for higher output load
Start up Time	T_osc	–	–	3	ms	Measured from the time Vdd reaches its rated minimum value
RMS Period Jitter	T_jitt	–	–	6	ps	f = 48 MHz, Vdd = 1.8 V
		–	–	4	ps	f = 48 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
RMS Phase Jitter (random)	T_phj	–	1.60	–	ps	f = 62.5 MHz, Integration bandwidth = 1.875 MHz to 20 MHz
		–	1.00	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz

**■ Dimensions, Pin Description and Land Pattern**

**Dimensions (Unit: mm)**

Note: XXXX top marking denotes manufacturing lot no.

**Recommended Land Pattern (Unit: mm)**

Note: A capacitor of value 0.1µF between Vdd and GND is recommended

**Pin #1 Functionality**

OE
H or Open; specified frequency output
L: output is high impedance
ST
H or Open; specified frequency output
L: output is low level (weak pull down)

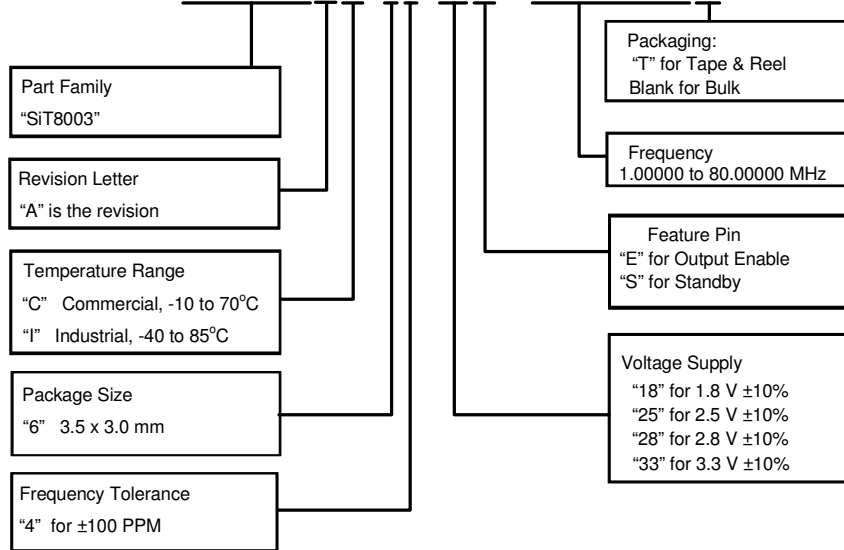
  

**Pin Map**

Pin	Connection
1	OE/ST
2	GND
3	CLK
4	VDD

**■ Part No. Guide- How to Order**

**SiT8003AC-64-18E - 123.12345T**



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