



MachXO Crossover Programmable Logic Devices



The MachXO family of crossover programmable logic devices (PLDs) combines CPLD and FPGA attributes together to optimally serve applications such as bus bridging, bus interface and control that traditionally were implemented in CPLDs or low capacity FPGAs. [More of the Best:](#) MachXO includes PLLs and embedded memory along with features you've come to expect in CPLDs.

Features

- ❖ **Non-Volatile Infinitely Reconfigurable**
 - Instant-on, powers up in less than 1mS
 - Single-chip, no external configuration memory
 - Excellent design security, no bit stream to intercept
- ❖ **Performance to 3.5ns Pin-to-Pin**
- ❖ **Available in Commercial, Industrial and AEC-Q100 Qualified Automotive Temperature Ranges**
- ❖ **TransFR™ Technology Allows Simple Field Upgrades**
- ❖ **Flexible LUT Architecture**
 - 256 to 2280 LUT4s
 - 73 to 271 I/Os with extensive package options
 - Density migration supported
- ❖ **Embedded and Distributed Memory**
 - Up to 27.6 Kbits sysMEM Embedded Block RAM
 - Includes dedicated FIFO control logic
 - Up to 7.7 Kbits distributed RAM
- ❖ **Programmable sysIO™ Buffer Wide Range of Interfaces Supports**
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTTL
 - PCI*
 - LVDS*, Bus-LVDS*, LVPECL*, RSDS*
- ❖ **sysCLOCK PLLs**
 - Up to two analog PLLs per device
 - Clock multiply, divide and phase shifting
- ❖ **Sleep Mode Reduces Standby Power to <100µA**
- ❖ **System Level Support**
 - IEEE Standard 1149.1 Boundary Scan
 - Onboard 20MHz oscillator for configuration and user logic
 - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

* MachXO1200 and 2280 devices only.



MachXO Evaluation Boards

Lattice offers two evaluation boards for MachXO devices. These boards provide ready-made platforms for evaluating the features and performance of the MachXO, or aiding in the development of your design.

MachXO-Starter Evaluation Board: This is a simple yet versatile board, featuring a MachXO-256 in a 100-TQFP package, on-board power, LEDs, and access to all device I/O. Each board includes an AC adapter and programming cable, giving you everything you need to get started designing with the MachXO in an affordable package. Software support is included in the downloadable version of ispLEVER-Starter.

MachXO-Standard Evaluation Board: This board features either a MachXO-640 or MachXO-2280 in a 256fpBGA package, multiple selectable voltage planes, on-board power, LEDs, access to all device I/O, prototyping area, and more.

MachXO Family Selection Guide

	LCMX0256	LCMX0640	LCMX01200	LCMX02280
V_{cc} Voltage (V)	1.2 or 1.8/2.5/3.3	1.2 or 1.8/2.5/3.3	1.2 or 1.8/2.5/3.3	1.2 or 1.8/2.5/3.3
Density LUTs	256	640	1200	2280
Density Macrocells¹	128	320	600	1140
tPD (ns)	3.5	3.5	3.6	3.6
Fmax (MHz)	388	388	388	388
Dist. RAM (Kbits)	2.0	6.0	6.25	7.5
EBR SRAM (Kbits)	0	0	9.2	27.6
EBR SRAM Blocks	0	0	1	3
PLLs	0	0	1	2
Maximum User I/O	78	159	211	271



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	LCMX0256	LCMX0640	LCMX01200	LCMX02280
100-pin TQFP (14x14 mm)	78	74	73	73
144-pin TQFP (20x20 mm)		113	113	113
100-ball csBGA (8x8 mm)	78	74		
132-ball csBGA (8x8 mm)		101	101	101
256-ball ftBGA (17x17 mm)		159	211	211
324-ball ftBGA (19x19 mm)				271

¹ Assumes 1 macrocell = 2 LUTs