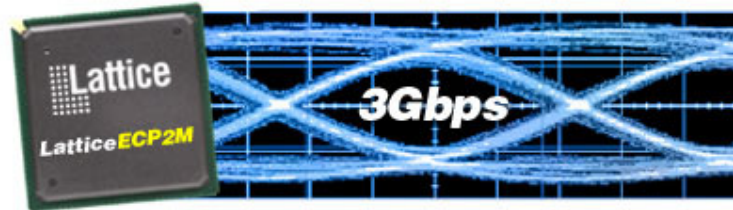


## LatticeECP2/M Low-Cost FPGA



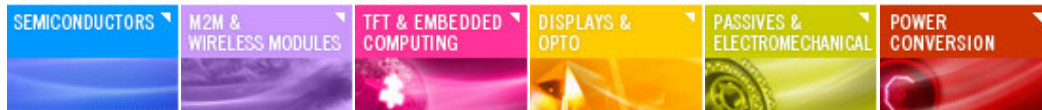
The LatticeECP2™ and LatticeECP2M™ families redefine the low-cost FPGA category, with [more of the best](#) FPGA features for less. By integrating features and capabilities previously only available on higher cost / high performance FPGAs, these families expand the range of applications that can take advantage of low cost FPGAs.

### Key Features

















- 4 to 16 SERDES - 3.125Gbps (ECP2M only)
  - Only 100mW power per channel
  - Supports PCIeexpress, Ethernet, & other packet protocols
- **Lowest Power SERDES-based FPGA**
  - 95K LUTs with under 0.35W static power
- **Optimized FPGA Architecture for Low Cost Applications**
  - Up to 5.3Mbit Block and Distributed RAM
  - Up to 95K LUTs
  - Up to 601 I/O
- **DSP Blocks**
  - With multiply, addition, subtract and accumulate
- **Pre-Engineered Source Synchronous I/O**
  - Supports up to 840Mbps LVDS I/O, DDR1/2 at 533Mbps , and SPI4.2 at 750Mbps
- **Superior Configuration Options**
  - Encrypted bitstream and dual boot support
  - TransFR technology for easy field upgrades

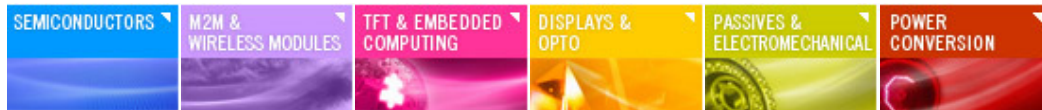
### Evaluation Boards and Design Support












- [ispLeverCORE Intellectual Property](#)
- [ispLEVER Design Tools](#)
- [LatticeECP2/M Applications](#)
- [LatticeECP2 Standard Evaluation Board](#)
  - To quickly evaluate the LatticeECP2 FPGA on a ready-made platform.



- [LatticeECP2 Advanced Evaluation Board](#)
  - Features more advanced interfaces for system-level evaluation and development.
- [LatticeECP2M PCI Express x4 Evaluation Board](#)
  - Provides a plug in card that can be used to evaluate the LatticeECP2M-50 (or LatticeECP2M-35) in PCI Express and generic SERDES applications.
- [LatticeECP2M SERDES Evaluation Board](#)
  - To evaluate the SERDES I/O of the LatticeECP2M-50 (or LatticeECP2M-35), interface to PCI Express x1, connect to SERDES via SFP or SATA, or for general SERDES applications.
- [LatticeECP2M SMPTE SDI Evaluation Board](#)
  - Part of a complete solution designed to demonstrate the integration of HD-SDI, SDI - SMPTE 259 and 292 - and DVB-ASI encoders and decoders into an FPGA.

LatticeECP2(including "S-Series") Selection Guide						
Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	56
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
DLL + PLL	2+2	2+2	2+2	2+2	2+4	2+6
Maximum Available I/O	190	297	402	450	500	583
Packages	I/O Count					
144-pin TQFP (20 x 20 mm)	90 	93 				
208-pin PQFP (28 x 28 mm)		131 	131 			
256-ball fpBGA (17 x 17 mm)	190 	193 	193 			
484-ball fpBGA (23 x 23 mm)		297 	331 	331 	339 	
672-ball fpBGA (27 x 27 mm)			402 	450 	500 	500 
900-ball fpBGA (31 x 31 mm)						583 



LatticeECP2M(including "S-Series") Selection Guide					
Device	ECP2M-20	ECP2M-35	ECP2M-50	ECP2M-70	ECP2M-100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL + SPLL + DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Packages	SERDES I/O Combinations				
256-ball fpBGA (17 x 17 mm)	4/140 	4/140 			
484-ball fpBGA (23 x 23 mm)	4/304 	4/303 	4/270 		
672-ball fpBGA (27 x 27 mm)		4/410 	8/372 		
900-ball fpBGA (31 x 31 mm)			8/410 	16/416 	16/416 
1152-ball fpBGA (35 x 35 mm)				16/436 	16/520 