GN4124 x4 PCI Express® to Local Bus Bridge

FEATURES

- 4 Lane PCI Express® interface
  - Complies with PCI Express Base Specification 1.1
  - On-chip PHY, transaction, and link layer eliminates the cost of IP licensing
  - 2 hardware virtual channels supported
  - Payload size of up to 512 bytes with up to 4 outstanding transactions in each direction
  - Supports 3-64 bit Base Address Registers
  - Provides flexible power management capability
- Provides pin efficient local bus interface for easy attachment to popular low-cost FPGA devices
  - Uses SSTL dual data rate I/O for high-speed data transfer (16 lanes and 800MB/s in each direction)
  - FPGA source code provided for 64 bit master/target read/write buses for easy user logic attachment
  - Local bus may be operated asynchronously to the PCIe clock rate for power optimization
- "Live" on power up
  - On-chip type 0 PCI configuration space enables auto detection without FPGA activity
  - On-chip extended configuration space supports power management, serial number, MSI, and PCIe capability registers
- FPGA bitstream loader
  - Allows easy configuration of the attached FPGA through PCIe
  - Provides on-the-fly FPGA reconfiguration capability
- I2C master/target
  - Master mode allows PCI configuration space defaults to be loaded from a small E^2PROM upon system reset
  - Target mode allows internal registers to be accessed from an external circuit
- 2kV ESD protection
- 256 pin 17mm x 17mm lead-free BGA
- <900mW power consumption during sustained operation
- 0-85°C operating temperature

APPLICATIONS

- High-speed data acquisition
- High definition video capture/playout
- Configurable computing
- Machine vision
- Networking and communications
- Migration to PCI Express

GENERAL DESCRIPTION

The GN4124 is a four lane PCI Express to local bus endpoint bridge that is designed to work as a companion for FPGA devices to provide a complete bridging solution for general applications. In addition to a 4-lane PCI Express compliant PHY interface, the GN4124 also contains the link and transaction layers, and an applications interface that is ideally suited to FPGA interfacing using a small number of pins.

Since the PCI Express transaction/link IP is hard-wired into the GN4124, there is no need to license PCIe IP. The level of integration and very low power operation of the GN4124 make it an ideal alternative to using a PIPE PHY, where IP licensing and the cost of FPGA resources and power consumption is unattractive by comparison. Using the GN4124 allows FPGA resources to be spent on what differentiates the product rather than on implementing the PCI Express protocol.

Live on Power-up

Since the GN4124 contains a complete type 0 PCI configuration space, it is live on power-up so that a plug-and-play BIOS can auto-detect it and enumerate it without an attached FPGA having to be configured.

FPGA *On-the-Fly* Configuration Loader

An FPGA configuration bitstream may be downloaded from the host system over PCIe to the attached FPGA using the on-chip FPGA Configuration Loader (FCL). This eliminates the expense of a dedicated FPGA ROM and makes on-the-fly reconfiguration and firmware upgrades simple. Any application requiring dynamic reconfiguration or firmware upgrades over PCIe can benefit from the use of the GN4124 as a companion device irrespective of the size or type of FPGA device used.

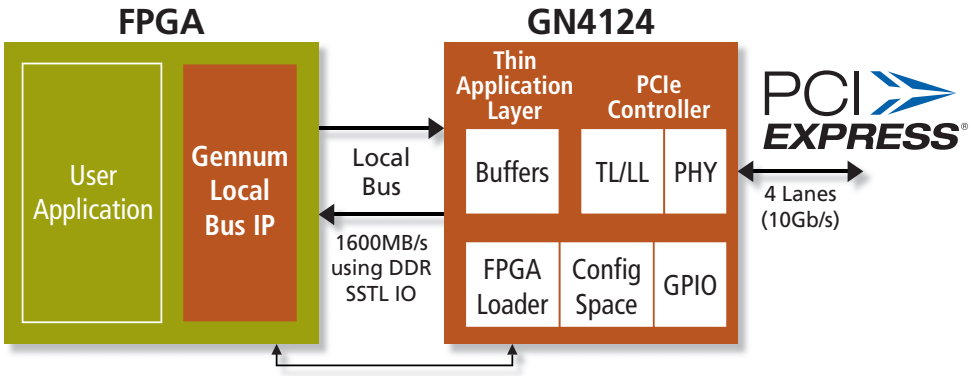
Local Bus Interface

The local bus interface uses a combination of single and dual data rate SSTL I/O to accomplish very high data rates using the fewest possible pins. A single data rate clock is used for SSTL control signals and separate dual data rate source synchronous clocking is used for the DDR SSTL data. The SDR control signals operate at up to 200MHz and the DDR I/O operate at up to 400MT/s across 16 bits using a 200MHz DDR clock. This provides 800MB/s in each direction. Optional on-chip termination may be enabled to enhance signal integrity and simplify board design.

The local bus may operate asynchronously from the PCI Express rate. In order to save power, the local bus clock can operate at the lowest possible rate required by an application.

The local bus protocol facilitates 4 types of transactions:

- PCIe-to-Local Target Writes: a PCIe agent (such as the host processor/root complex) writes data to the local bus.



GN4124 Simplified Block Diagram

- PCIe-to-Local Target Reads: a PCIe agent reads data from the local bus. Reads are split into a request phase (address phase) and a completion phase (data phase)
- Local-to-PCIe Master Writes: the attached FPGA writes data to a PCIe device (such as host memory).
- Local-to-PCIe Master Reads: the attached FPGA reads data from a PCIe device.

The PCIe-to-Local transactions would typical involve a target controller implemented in the FPGA. Local-to-PCIe Master transactions allow a DMA controller in the FPGA to access PCI Express devices.

Virtual Channel Support

The GN4124 has 2 independent virtual channels that support the 8 PCIe defined traffic classes. This enables high local bus utilization by supporting non-blocking traffic between virtual channels. This is accomplished with separate on-chip buffering resources for each of the two virtual channels. For example, when write buffering is full for VC0 and VC1 has room, then VC1 traffic may proceed without reference to the state of VC0.

Virtual channels may be used to separate different types of application traffic. For example, a DMA engine in the FPGA may be aggressively reading and writing host memory to stream video data. At the same time another agent in the FPGA may need to communicate low bandwidth, latency sensitive synchronization information. If the two types of traffic are segregated in terms of virtual channels and traffic classes, then the low latency traffic can be allowed to pass the high bandwidth traffic.

PCI Express Application Layer

The on-chip applications layer transfers data between the PCI Express port and an attached FPGA using the local bus interface. It also provides a mechanism to access internal registers through configuration space access and through one of the Base Address Registers (BAR4). The applications layer also supports the transmission of message signalled interrupts.

Interrupt Controller

A flexible interrupt controller automatically generates PCIe message signalled interrupts from either external pins (GPIO pins) or internally generated interrupt sources. In addition, the interrupt controller can route any interrupt source to up to 4 GPIO pins.

2-wire Serial Controller

An on-chip I^2C compatible "2-wire" controller provides both a master and target mode. After device reset "boot master mode" is optionally initiated so that default configuration register values, such as Subsystem Vendor ID and BAR sizes, can be automatically loaded from a small serial EEPROM.

After initialization, target mode allows an external 2-wire master to access on-chip registers. The 2-wire master mode controller in the GN4124 can be accessed over PCI Express to access external 2-wire target devices.

GENERAL PURPOSE IO

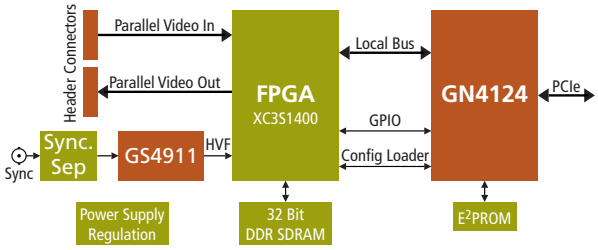
Sixteen General Purpose IO pins are available for user applications. They may be used as inputs or outputs. A subset may be used for interrupt inputs.

COMPLETE SOLUTION

Gennum provides a complete solution around the GN4124 to accelerate your design cycle. This includes full documentation, an evaluation board with schematics, FPGA local bus interface IP, example FPGA application code, driver software, and example application software.

Reference Design Kit

The GN4124 RDK consists of the "Gullwing" RDK board, DMA benchmarking FPGA firmware and GenDiag application software. Out of the box, the Gullwing RDK board can be run on a PC platform with the supplied IP and software to measure actual performance on specific hardware platforms.

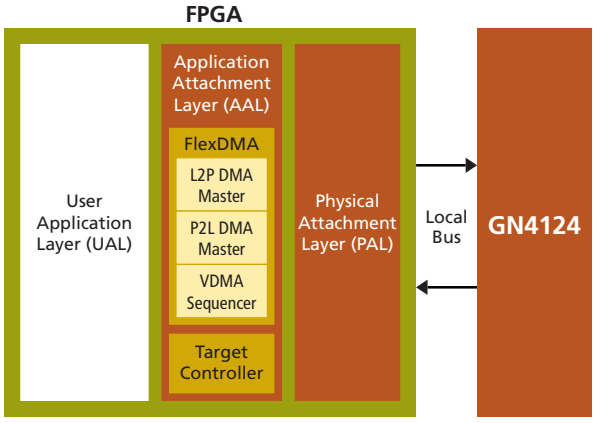


Gullwing Board Simplified Block Diagram

Local Bus FPGA IP

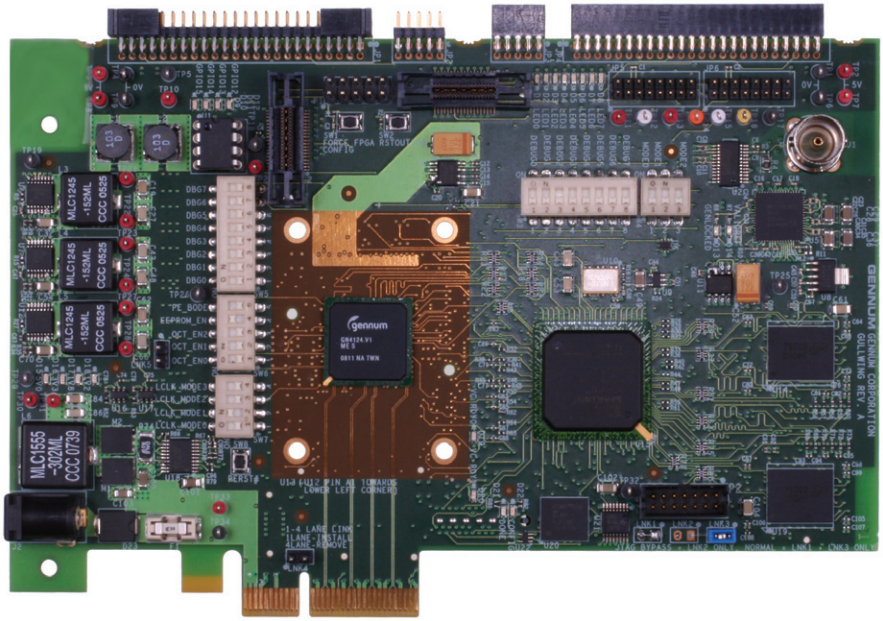
In order to simplify design, Gennum provides FPGA IP for interfacing to the Local Bus of the GN4124. It uses a layered approach so that part or all of the IP may be used. The layers are:

- Physical Attachment Layer (PAL): provides the interface to the GN4124 taking the high-speed, narrow external buses and widening them out for use inside the FPGA
- Application Attachment Layer (AAL): provides a target interface and the FlexDMA master mode DMA block.
- User Application Layer (UAL): the local bus core ships with a benchmarking application layer. However, this is easily replaced by the users application.



Gennum Supplied Local Bus FPGA IP

The local bus FPGA IP is licensed, and royalty free for use with the GN4124.



Gullwing RDK Board for the GN4124

FlexDMA FPGA IP Core

The FlexDMA core is an integral part of the Application Attachment Layer of the Local Bus IP and comprises 3 main blocks:

- L2P DMA Master: Local-to-PCIe raw DMA engine
- P2L DMA Master: PCIe-to-Local raw DMA engine
- VDMA Sequencer: manages and virtualizes the raw DMA engines, provides scatter/gather capability

The L2P DMA master performs all DMA in the local to PCIe direction. For this, data is sourced from the application layer and written into host memory. Up to 256 sources may be used with the L2P DMA master under the control of the VDMA sequencer. The P2L DMA master operates concurrently for data flow in the PCIe to local direction and also supports up to 256 channels.

The role of the VDMA sequencer is to manage both the L2P DMA master and P2L DMA master. It uses SRAM in the FPGA to store descriptors. The descriptors are simple instructions used to interpret scatter/gather lists.

Scatter/gather lists consist of a series of DMA information including host address, transfer length, DMA direction, and application layer stream select information. The host side driver may queue up a scatter/gather list for the VDMA sequencer to process independently. This reduces overhead on the host system.

GenDiag Application Software

The GenDiag software is a command line interface that can be used to configure and exercise the Gullwing RDK board. GenDiag provides capabilities to:

- Find and attach to the Gullwing RDK board in the host computer
- Dump the contents of the internal registers inside the GN4124 and inside the FPGA attached to the GN4124
- Read and write registers inside the GN4124
- Read and write registers and memory inside the FPGA on the Gullwing card
- Program the FPGA on the Gullwing card from a file over the PCI Express link
- Run the DMA benchmarking application
- Perform board diagnostics

Source code is available for GenDiag to use as a starting point for user programming.

GenDiag uses the WinDriver® product, available from Jungo, to provide all kernel mode hardware access. Consequently, GenDiag is written as a user mode driver and application. WinDriver supports Windows 2000 / XP / XP Embedded / Server 2003, Vista, Windows CE / Mobile, Linux, Solaris and VxWorks. GenDiag, or any driver/application written using WinDriver, can be used on all of these same operating systems. More information on WinDriver is available from:

www.jungo.com

UPDATES

Updates to FPGA IP, software, schematics, and other design files is available through the MyGennum portal at:

www.gennum.com/mygennum

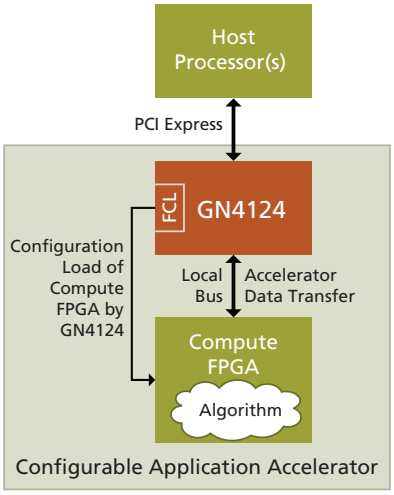
MyGennum resources are available to qualified registered users.

EXAMPLE APPLICATIONS

Due to the general purpose nature and flexibility of the GN4124, many applications can be supported.

Configurable Computing

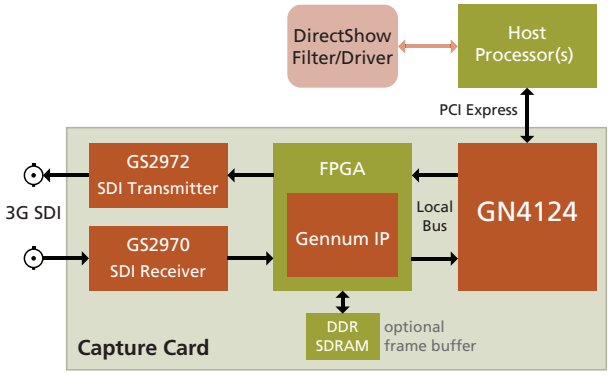
With an on-chip FPGA Configuration Loader (FCL), the GN4124 enables configurable computing applications that use FPGA to implement algorithms. The FCL supports all mainstream low-cost and feature rich FPGA families. Efficient data interchange between the host CPU and the accelerator is assured by the high-throughput local bus interface on the GN4124. The FlexDMA FPGA IP from Gennum simplifies the attachment of the application accelerator block to the system.



GN4124 Used in Configurable Computing Application

HD Video Capture

By combining the GN4124 PCI Express-to-local bus endpoint bridge with the GS297x family of SMPTE compliant SDI receivers/transmitters, HD video capture and playout is achieved. To further accelerate time-to-market for this application, Gennum provides FPGA IP and example DirectShow filter driver code to help accelerate development.

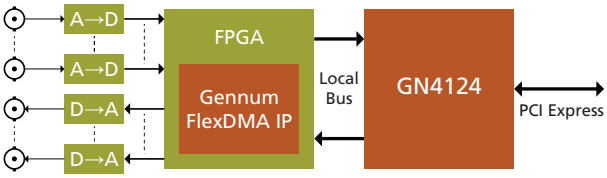


HD Video Capture Using the GN4124

The GN4124 has enough bandwidth to accommodate multiple channels of HD video including 1080p50/60. Other video I/O types such as HDMI or analog formats can be accommodated by changing the video I/O chips.

Data Acquisition

Data acquisition over PCI Express is easily implemented with the GN4124 and the FlexDMA FPGA IP core. The FlexDMA IP core from Gennum supports up to 256 channels of scatter/gather DMA in each direction (512 total). Since the GN4124 provides full duplex traffic via the local bus, simultaneous inputs and outputs can take advantage of the full duplex nature of PCI Express.

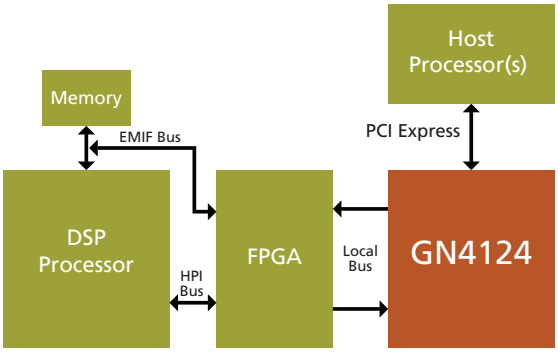


Data Acquisition Using the GN4124

DSP Based Accelerator via PCI Express

Using the GN4124 and a low-cost FPGA, interfacing DSP processors to PCI Express is simplified. Either the External Memory Interface (EMIF) or Host Processor Interface (HPI) (or both) may be used as the access point to the DSP. The FlexDMA FPGA IP core provided by Gennum provides a DMA master interface and target interface. Using the EMIF interface, the target controller of the Gennum FPGA IP can be used to map DSP memory into the address space of the host controller. This same approach can be used to map the HPI interface into host address space.

For high-bandwidth, low host processor overhead data movement, the scatter/gather master mode DMA of the FlexDMA IP can be used to shuttle data between the host and EMIF/HPI interfaces.



DSP Interfacing with the GN4124

ABOUT GENNUM

Gennum Corporation (TSX: GND) designs innovative semiconductor solutions and intellectual property (IP) cores for the world's most advanced consumer connectivity, enterprise, video broadcast and data communications products. Leveraging the company's proven optical, analog and mixed-signal products and IP, Gennum enables multimedia and data communications products to send and receive information without compromising the signal integrity. An awardwinner for advances in high definition (HD) broadcasting, Gennum is headquartered in Burlington, Canada, and has global design, research and development and sales offices in Canada, Mexico, Japan, Korea, Germany, United States, Taiwan, India and the United Kingdom.

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