

Digital Automotive Pixel Link

APIX is a new serial GBit/s link for DISPLAY and CAMERA based point-to-point applications. It features unidirectional pixel and full-duplex sideband data transmission over one single pair of shielded twisted pair (STP) copper cable. Alternatively an Automotive optimized operation mode with two pairs of STP is possible, where one pair is used for the 1Gbit/s Pixel link and the downstream Sideband and the other pair is used for the upstream Sideband and potentially the power supply.

APIX also supports transmission over fiber optic cable.

The APIX link is designed for the direct connection of high resolution TFT displays and CMOS image sensors to central graphic and image processors. The parallel interface of the APIX devices can be configured individually to match all popular display and image sensor interfaces.

Featuring a unique, asynchronous clock system, APIX links can also be cascaded to form loss-free distributed video networks in the car. Dedicated high-speed outputs with adjustable drive current and pre-emphasis in combination with spread-spectrum clocking facilitate the adaptation to different link distances and cable qualities while offering maximum data integrity and full EMI compliance.

Features:

- Up to 1 GBit/s Downstream Link Bandwidth
- Up to 62.5 MBit/s max Upstream Link Bandwidth
- Low EMI, Two- or Four-Wire Full Duplex Link
- +15 m Distance with low profile STP cables
- Tx/Rx: 10/12/18/24 bit RGB Interface
- DC-balanced line coding to support AC coupling
- Line Driver Current and Pre-Emphasis adjustable
- MicroWire[®] compatible Interface for Link configuration
- Extended Temperature Range: -40 to +105°C
- AEC-Q100

INAP125T12
INAP125T24
INAP125R12
INAP125R24

In addition to this datasheet it is highly recommended to consider further APIX documentation. Reference schematic and layout data are available on request. Please contact technical support.

Packages:

- 48 pin QFN (Quad-Flat No-Leads)
- 52 pin QFN
- 64 pin QFN

Applications:

- Automotive Infotainment Displays
- Automotive Dashboard Displays
- Head-Up Displays
- Rear-Seat Entertainment Systems
- Automotive Driver Assistance
 - Lane Departure Warning
 - Blind Spot Detection
 - Sign Recognition
 - Rear View
 - Night Vision
 - Passenger Occupancy
- Surveillance Systems
- Machine Vision
- Inspection Systems

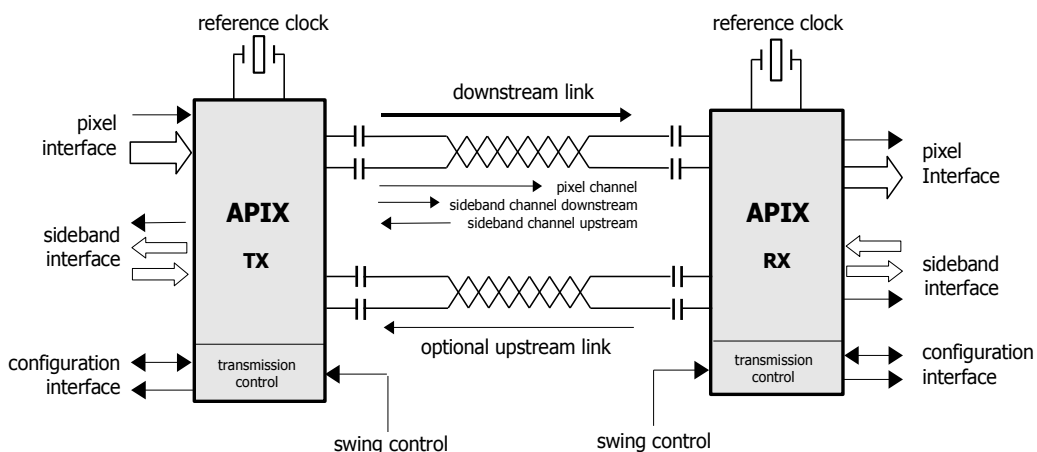


Figure 1: APIX Pixel Link Overview

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1 Introduction

The APIX link transmits uncompressed pixel data with a sustained and resolution-independent data rate of 1 GBit/s (500 MBit/s) over one single pair of STP copper cable. In addition to the pixel data, bi-directional sideband control data can be transmitted over the same pair of cable.

The link supports distances of up to +15m (1 GBit/s mode) and up to +40m+ (500 MBit/s mode) depending on the output settings (current, pre-emphasis) and the cable properties.

The APIX chip features a flexible interface that can be configured for specific applications. These include the camera link from CMOS image sensors to a display/image processing unit, or the display link from a graphics processor to displays in the dashboard or rear seats.

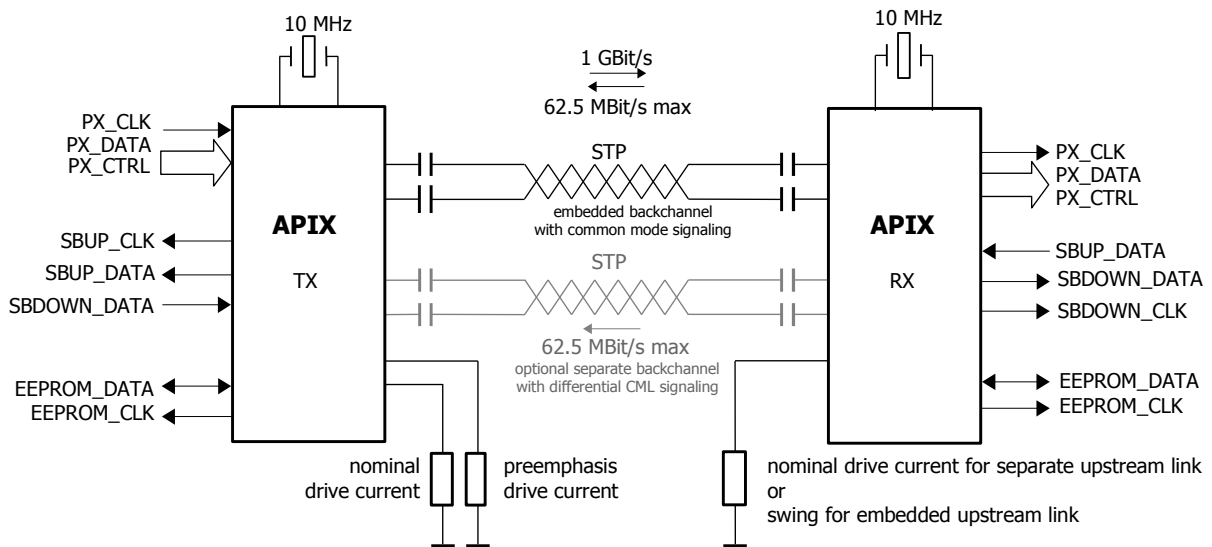


Figure 2: APIX Link Interfaces & Controls

1.1 Link Bandwidth

The physical connection between the Tx and Rx APIX devices is established by a single pair of STP copper cable carrying the downstream channels (pixel and control data) and the upstream channel (control data).

As an option, the APIX devices can also be configured to transmit the upstream data (back channel) over a separate pair of STP copper cable.

The bandwidth of the downstream link can be selected from these two modes:

- "full bandwidth" mode with a link data rate of 1 GBit/s for high-resolution, full color display links
- "half bandwidth" mode with a link data rate of 500 MBit/s for camera links, or small-size displays

The upstream link provides a link data rate of 62.5 MBit/s, 41.7 MBit/s, 31.3 MBit/s or 20.8 MBit/s (see table 6 + 7).

1.2 Transmission Channels

The APIX link provides three independent channels for data transfer: the uni-directional pixel channel (1 x downstream) and the bi-directional sideband channels for control data (1 x downstream, 1 x upstream).

The pixel channel and the downstream sideband channel are multiplexed and commonly transmitted over the downstream link.

The upstream sideband channel can either be established over the same pair of cable as the downstream link (embedded return channel) or alternatively over a separate pair of cable.

Channels	1 GBit/s Mode	500 MBit/s Mode
Downstream	maximum pixel clock frequency	Maximum pixel clock frequency
10 bit px_data	62.0 MHz	31.0 MHz
12 bit px_data	61.0 MHz	30.5 MHz
18 bit px_data	42.0 MHz ^{Note 1}	21.0 MHz ^{Note 1}
24 bit px_data	32.0 MHz	16.0 MHz
Sideband Channel	2 x 1 bit sampled ^{Note 2}	
Upstream		
Sideband Channel	2 x 1 bit sampled ^{Note 2}	

Table 1: Bandwidth of upstream/downstream channels

Note 1: To achieve 42.0 Mhz / 21 MHz pixel clock frequency with 18 Bit pixel data the "control signal transmit mode" has to be set to '10' (please refer to configuration tables page 10 and 11)

Note 2: Side band channels' up- and downstream bandwidths are fixed. The side band channel bandwidth is independent of the actual pixel clock frequency. For further informations about the side band capabilities please refer to chapter 2.

2 APIX Transmitter

2.1 Functional Block Diagram

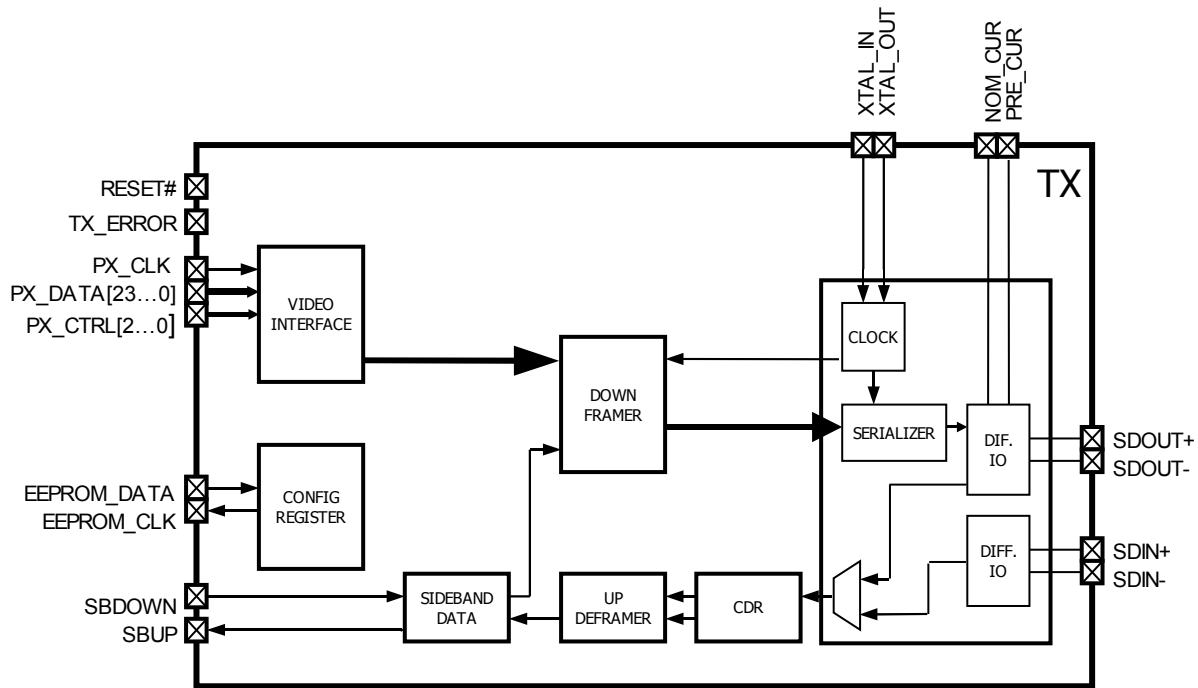


Figure 3: Tx Functional Overview

2.2 Interfaces

2.2.1 Downstream Link Interface

The interface (SDOUT+, SDOUT-) of the downstream serial link (Tx -> Rx) is implemented as differential Current Mode Logic (CML).

2.2.2 Upstream Link Interface

As the upstream serial channel (from Rx to Tx) can alternatively be established over the downlink (embedded back channel) or a separate pair of STP cable, different signalling techniques will be employed.

Option 1: Upstream and downstream channels share the same pair of STP cable. The upstream link employs common mode signalling technique.

Option 2: Upstream and downstream channels are transmitted over 2 separate pairs of STP cable. The additional upstream interface of the APIX devices (SDIN+, SDIN-) is realized with differential Current Mode Logic (CML).

2.2.3 Pixel Channel Interface

Up to 24 bit of parallel pixel data representing the pixel RGB values is received via the pixel interface. The parallel pixel interface supports pixel formats of 10, 12, 18 and 24 bit + 3 control signals. Pixel data and control signals are combined with the pixel interface clock. The active edge can be configured to either rising or falling. The logic level of this interface is 3.3 V.

2.2.4 Sideband Channel Downstream Interface

The side band data downstream interface provides one 2-bit wide data input* where 2 bits of data are sampled. Sample frequency depends on the serial bit rate.

Downstream speed	Sample frequency	Max. jitter of sampled data	Number of asynchronous channels
1 GBit/s full bandwidth mode	13,89 MHz	80 ns	2 *
500 MBit/s half bandwidth mode	6,94 MHz	160 ns	2 *

2.2.5 Sideband Channel Upstream Interface

The sideband data upstream interface provides one 2-bit wide data output* where 2 bits of data are provided together with the corresponding clock (interface timing chapter 5.1.5.2).

Note: * Depending on the APIX device used, -only one 1-bit side band channel may be available (see chapter 7 “Package Options”).

2.2.6 Signal Description

Signal Name	Direction	Description
PX_DATA[23...0]	IN	Max 24 bit of pixel data: 10 bit mode: PX_DATA[9...0]; 12 bit mode: PX_DATA[11...0] 18 bit mode: PX_DATA[17...0]; 24 bit mode: PX_DATA[23...0]
PX_CLK	IN	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of PX_CLK.
PX_CTRL[2...0]	IN	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid. Displays: PX_CTRL[0]: HSYNC; PX_CTRL[1]: VSYNC; PX_CTRL[2]: DATA_ENABLE
SBDOWN_DATA[1...0]	IN	Data sideband channel downstream
SBUP_DATA[1...0]	OUT	Data sideband channel upstream
SBUP_CLK	OUT	Sideband channel upstream clock
RESET#	IN	Asynchronous reset (active low)
TX_ERROR	OUT	Upstream Link Sync Error Indicator (active high)
EEPROM_DATA	IN/OUT	Configuration data
EEPROM_CLK	OUT	Configuration clock
XTAL_IN	IN	Oscillator input or reference clock input
XTAL_OUT	OUT	Oscillator output
NOM_CUR	PASSIV	Serial data downstream: nominal current control
PRE_CUR	PASSIV	Serial data downstream: pre-emphasis current control
SDOUT+	OUT	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDOUT-	OUT	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDIN+	IN	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDIN-	IN	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
VDD_VCO	IN/PWR	Regulated power supply for VCO 1.8 V, 7 mA
VCO_TUNE	IN	VCO loop filter tuning voltage
PFD_OUT	OUT	Current output for VCO loop filter
VDD	PWR	1.8 V core supply
DVDD	PWR	3.3 V I/O supply
VSS	PWR	Digital core ground
DVSS	PWR	Digital I/O ground
VDDA	PWR	1.8 V analog supply
GND_A	PWR	Analog ground
VDD_OSC	PWR	1.8 V oscillator supply
DVDD_OSC	PWR	3.3 V oscillator supply
VSS_OSC	PWR	Oscillator ground
DVSS_OSC	PWR	Oscillator I/O ground

Table 2: Transmitter signal description

3 APIX Receiver

3.1 Functional Block Diagram

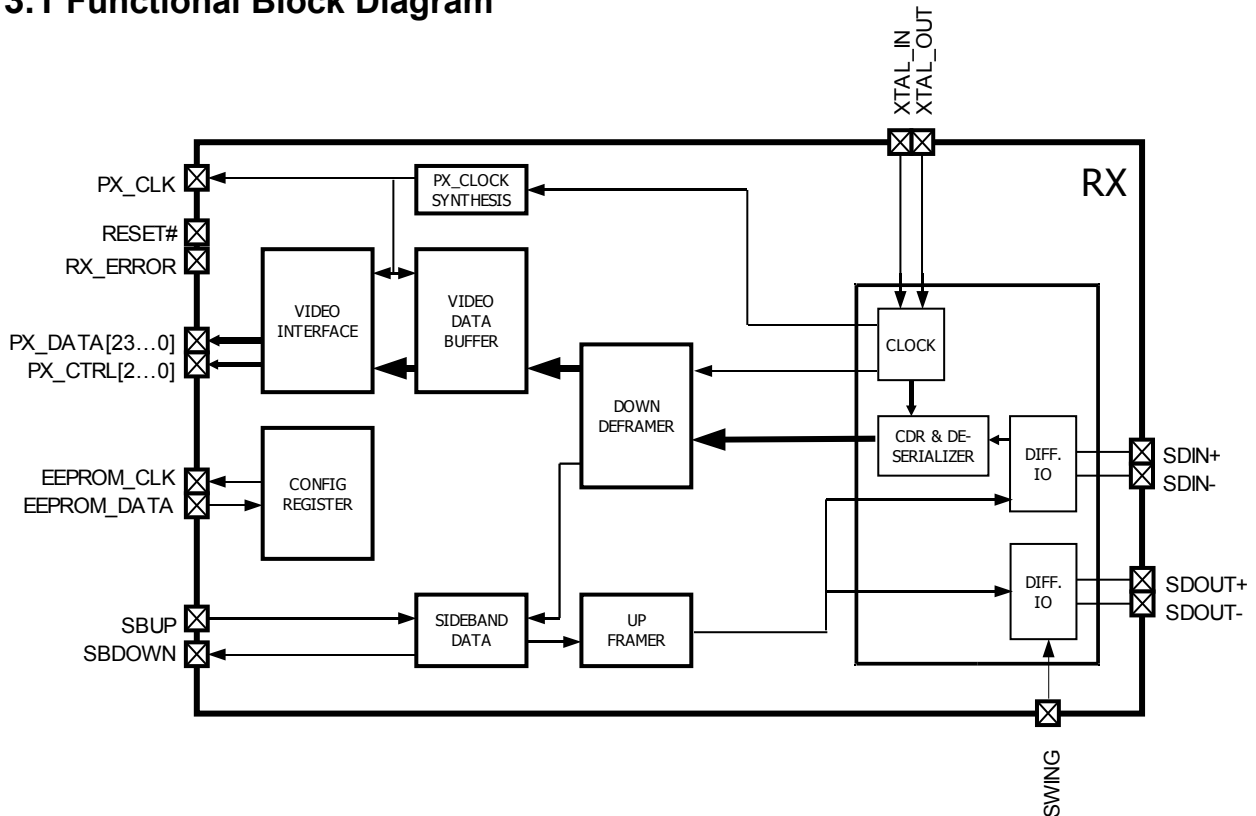


Figure 4: Rx Functional Overview

3.2 Interfaces

3.2.1 Downstream Link Interface

The input of the serial link (SDIN+, SDIN-) is implemented as Current Mode Logic (CML). An analog equalizer is provided to pre-process the incoming serial signal.

3.2.2 Upstream Link Interface

APIX offers two options to establish the upstream link (see 2.2.2). The upstream link can also be fully disabled.

3.2.3 Pixel Channel Interface

Up to 24 bit of parallel pixel data representing the pixel RGB values are provided at the pixel interface. The parallel pixel interface supports pixel formats of 10, 12, 18 and 24 bits + 3 control signals. Pixel data and control signals are provided with reference to the pixel interface clock. The active edge can be set to either rising or falling. Pixel clock jitter is better than 1 ns. The interface has 3.3 V CMOS logic levels.

3.2.4 Sideband Channel Downstream Interface

The side band data downstream interface provides one 2-bit wide data output* where 2 bits of data are provided together with the corresponding clock (interface timing chapter 5.1.5.1) .

3.2.5 Sideband Channel Upstream Interface

The side band data upstream interface provides one 2-bit wide data input* where 2 bits of data are sampled.

Upstream serial line clock	Sample frequency	Max. jitter of sampled data	Number of asynchronous channels
62,5 MHz	10,41 MHz	104 ns	2 *
41,67 MHz	6,94 MHz	152 ns	2*
31,25 MHz	5,21 MHz	200 ns	2 *
20,83 MHz	3,47 MHz	304 ns	2 *

Note: * Depending on the APIX device used, only one 1-bit sideband channel may be available (see chapter 7 “Package Options”).

3.2.6 Signal Description

Signal Name	Direction	Description
PX_DATA[23...0]	OUT	Max 24 bit of pixel data if parallel mode: 10 bit mode: PX_DATA[9...0]; 12 bit mode: PX_DATA[11...0] 18 bit mode: PX_DATA[17...0]; 24 bit mode: PX_DATA[23...0]
PX_CLK	OUT	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of PX_CLK (parallel mode)
PX_CTRL[2...0]	OUT	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid. Displays: PX_CTRL[0]: HSYNC; PX_CTRL[1]: VSYNC; PX_CTRL[2]: DATA_ENABLE
SBUP_DATA[1...0]	IN	Data sideband channel upstream
SBDOWN_DATA[1...0]	OUT	Data sideband channel downstream
SBDOWN_CLK	OUT	Sideband channel downstream clock
RESET#	IN	Asynchronous reset (active low)
RX_ERROR	OUT	Error Indicator: PX_CLK error, or down link sync error (active high)
EEPROM_DATA	IN/OUT	Configuration data
EEPROM_CLK	OUT	Configuration clock
XTAL_IN	IN	Oscillator input or reference clock input
XTAL_OUT	OUT	Oscillator output
PX_VCO_IN	IN	VCO for pixel clock generation – Input
PX_VCO_OUT	OUT	VCO for pixel clock generation – Output
SWING	PASSIV	Upstream channel: nominal current control
SDOUT- SDOUT+	OUT OUT	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDIN+ SDIN-	IN IN	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
VDD_VCO	IN/PWR	Regulated power supply for VCO 1.8 V, 7 mA
VCO_TUNE	IN	VCO loop filter tuning voltage
PFD_OUT	OUT	Current output for VCO loop filter
VDD	PWR	1.8 V core supply
DVDD	PWR	3.3 V I/O supply
VSS	PWR	Digital core ground
DVSS	PWR	Digital I/O ground
VDDA	PWR	1.8 V analog supply
GNDA	PWR	Analog ground
VDD_OSC	PWR	1.8 V oscillator supply
DVDD_OCS	PWR	3.3 V oscillator supply
VSS_OSC	PWR	Oscillator ground
DVSS_OSC	PWR	Oscillator I/O ground

Table 3: Receiver signal description

4.1.2 Rx device configuration vectors

Address (hex)	Bit #	Parameter	Recommended configuration value	Default configuration value	Comment
00	7:0	PROM_start	1011_1101		PROM valid byte 0
01	0	reserved	1		
	1	pixel interface wake-up 1		0	0: force pixel interface to "0" until VCO is stable 1: pixel interface is always enabled
	2	reserved	1		
	3	dedicated upstream		1	0: disable 1: enable dedicated upstream link Note: in case bits 3 and 4 are set to '1', the upstream channel is disabled
	4	embedded upstream		0	0: disable 1: enable Note: in case bits 3 and 4 are set to '1', the upstream channel is disabled
	5	reserved	0		
	6	bandwidth mode		1	0: 1 GBit/s mode 1: 500 MBit/s mode
	7	wait period after configuration	1(MSB)	1	0: no delay 1: 50 ms delay after configuration to stabilize the PLL
02	1:0	pixel data width		00	00: 10 bit 01: 12 bit 10: 18 bit 11: 24 bit
	3:2	control signal transmit mode	11	11	configure transmission of pixel control signals 00: never; 01: unused; 10: on every second (even) pixels; 11: on each pixel
	4	reserved	1		
	5	pixel clock active edge		1	0: falling edge 1: rising edge
	7:6	upstream link serial clock		01	For detailed information refer to chapter 4.1.3
03	0	reserved	0		
	1	pixel interface wake-up 2	0 *	0	PX_DATA and PX_CTRL start at the upper left corner 0: disable 1: enable
	2	pixel interface wake-up 3	0 *	0	PX_CLK starts at the upper left corner 0: disable 1: enable
	3	fault tolerant transmission	1	1	tolerates single bit errors within the timing window 0: disable 1: enable
	7:4	reserved	0000		
04	0	pll status	0	0	0: loss of PLL synchronization resets device 1: disable
	7:1	reserved	0000110		
05	7:0	reserved	00000001		
06	7:0	reserved	00000000		
07	7:0	PROM_end	1001_1001		PROM valid byte 1

Table 5: Configuration of the Rx device

Note: The APIX receiver chip starts in default mode, if invalid PROM_start or PROM_end are received. Default configuration values for APIX receiver are listed at table 5.

* The pixel interface wake-up function is an option for displays only. It requires a valid video timing with all three control signals HSYNC (CTRL0), VSYNC (CTRL1) and DE (CTRL2) for proper function.

4.1.3 Configuration of the Sideband Upstream Channel's Clock System

The sideband upstream interface supports different levels of transmission bandwidth selected through configuration settings. The following descriptions are always valid, no matter if the embedded (= one-pair cable link) or external (= two-pair cable link) upstream channel is used.

4.1.3.1 Configuration for 1 GBit/s Full Bandwidth Mode

Bandwidth mode	Tx upstream link serial clock	Rx upstream link serial clock	Upstream serial clock speed
1 GBit/s	00	01	62.5 MHz
1 GBit/s	01	10	41.67 MHz
1 GBit/s	10	11	31.25 MHz

Table 6: Sideband upstream configuration for full bandwidth mode

4.1.3.2 Configuration for 500 MBit/s Half Bandwidth Mode

Bandwidth mode	Tx upstream link serial clock	Rx upstream link serial clock	Upstream serial clock speed
500 MBit/s	00	00	62.5 MHz
500 MBit/s	10	01	31.25 MHz
500 MBit/s	11	10	20.83 MHz

Table 7: Sideband upstream configuration for half bandwidth mode

4.1.4 Configuration procedure

For the configuration of all parameters, the APIX device provides a MicroWire™ compatible two-wire interface and supports MicroWire™'s sequential read operation. Recommended EEPROMs are e.g. 93L46A or 93L46C by Microchip Technology Inc. with selected word size 8 bit. The MicroWire™ protocol can be also implemented with any microcontroller utilizing general purpose IOs. The following diagram provides the configuration flow:

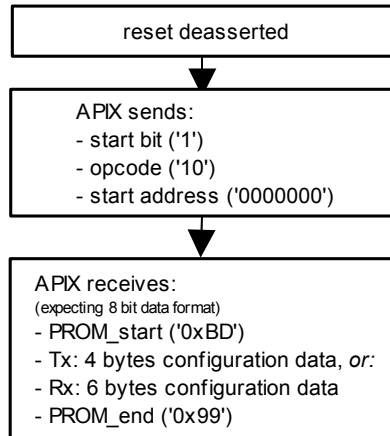


Figure 5: Configuration flow

Note: In case of invalid “PROM_start” or “PROM_end” bytes, default configuration is used (see chapter “Configuration Settings”).

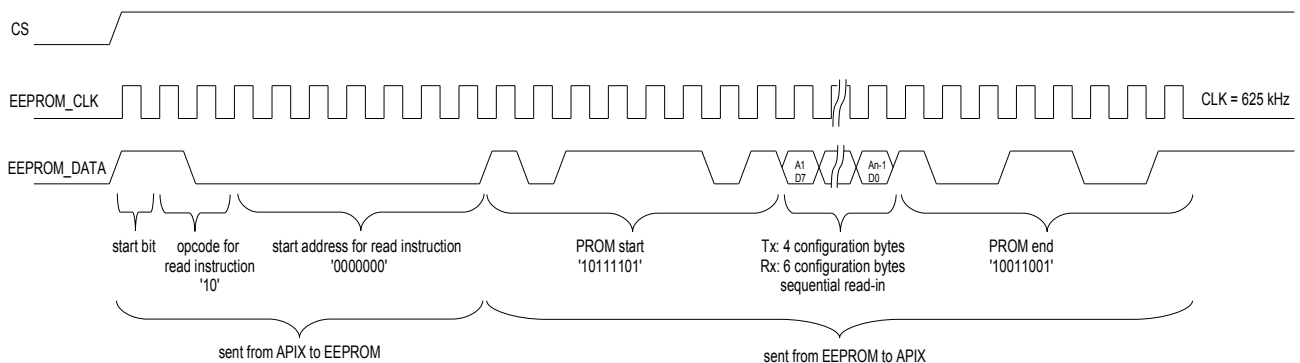


Figure 6: Configuration sequence

Note: Each individual configuration byte is read in starting from bit 7 towards bit 0. APIX samples all bits at falling edge of EEPROM_CLK.

The following schematic shows an external configuration circuitry using EEPROM 93LC46A-P:

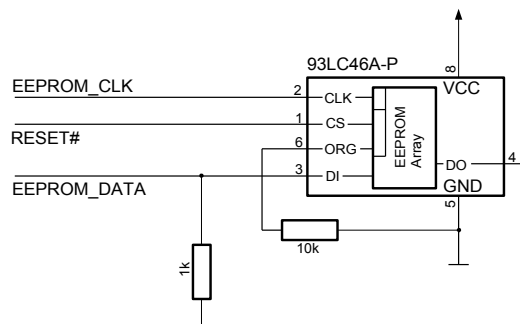


Figure 7: External configuration circuitry

4.2 Reset

Asynchronous reset (active low) can be activated at any time and sets the devices into a defined state. The minimum low pulse width is four reference clock cycles (ref clock specification Table 22).

During reset serial output pins SDOOUT-, SDOOUT+ are hold on VDDA level. All parallel outputs pins are at low level. EEPROM_DATA is set to Hi-Z (both Tx and Rx).

4.3 Power-Up

4.3.1 Power-Up Sequence

It is mandatory to power all 1.8V supplies (VDD, VDDA, VDD_VCO, VDD_OSC) at the same time. There is no special power-up sequencing required for DVDD (3.3V)

4.3.2 Power Supply Filtering

To achieve best transmission performance a noise level of less than 50mV on all analog and digital supply voltages VDD, VDDA, VDD_VCO, VDD_OSC and DVDD is recommended. Please consider also APIX reference schematic and layout data which are available on request.

4.3.3 PLL-Lock-Time

The PLL-Lock-Time is less than 5 ms.

4.4 Error Detection

4.4.1 Tx Error Signaling

Signal TX_ERROR goes high if there is an upstream link sync error.

4.4.2 Rx Error Signaling

Signal RX_ERROR goes high if there is a pixel clock error *or* a down link sync error.

5 Electrical Specification

5.1 Timing Parameters & Diagrams

5.1.1 Tx Pixel Interface / Rising Edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Pixel data and control signal setup time to pixel clock at Tx	1.5	2	-	ns
t_2	Pixel data and control signal hold time to pixel clock at Tx	-	0	1	ns

Table 8: Pixel Interface Timing Table at Tx Pixel Interface / Positive Edge

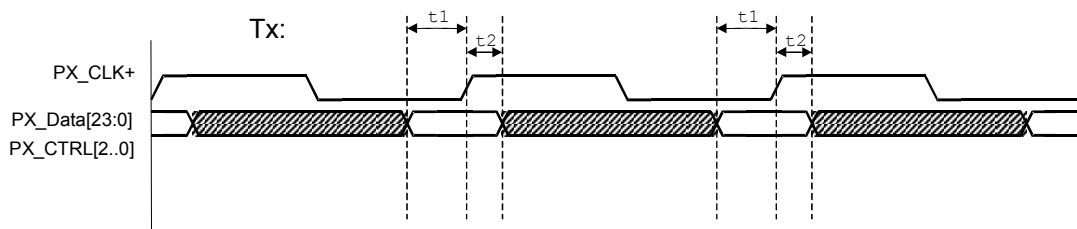


Figure 8: Tx Pixel interface timing diagram at rising edge

5.1.2 Rx Pixel Interface / Rising Edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_3	Pixel data and control signal setup time to pixel clock at Rx	2.6	3	3.5	ns
t_4	Pixel data and control signal hold time to pixel clock at Rx	1.8	2	2.5	ns

Table 9: Pixel Interface Timing Table at Rx Pixel Interface / Positive Edge

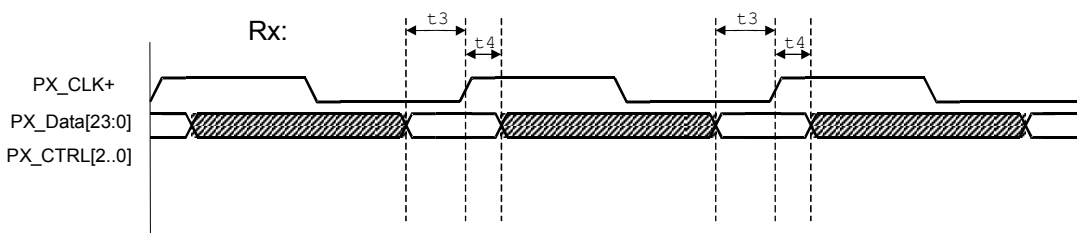


Figure 9: Rx Pixel interface timing diagram at rising edge

5.1.3 Tx Pixel Interface / Falling Edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_5	Pixel data and control signal setup time to pixel clock at Tx	1.5	2	-	ns
t_6	Pixel data and control signal hold time to pixel clock at Tx	-	0	1	ns

Table 10: Pixel Interface Timing Table at Tx Pixel Interface / Negative Edge

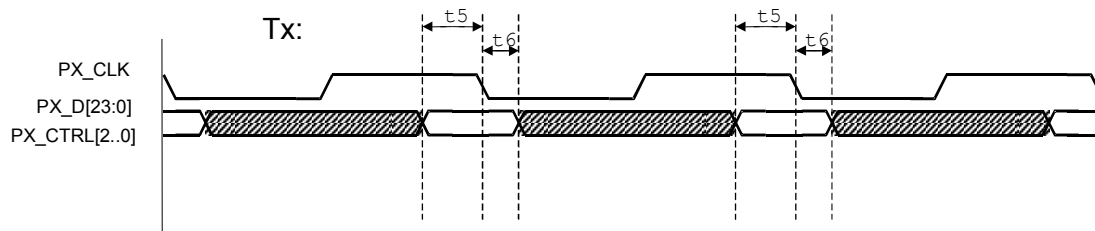


Figure 10: Tx Pixel interface timing diagram at falling edge

5.1.4 Rx Pixel Interface / Falling Edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_7	Pixel data and control signal setup time to pixel clock at Rx	2.3	2.4	3	ns
t_8	Pixel data and control signal hold time to pixel clock at Rx	1.8	1.9	2	ns

Table 11: Pixel Interface Timing Table at Rx Pixel Interface / Negative Edge

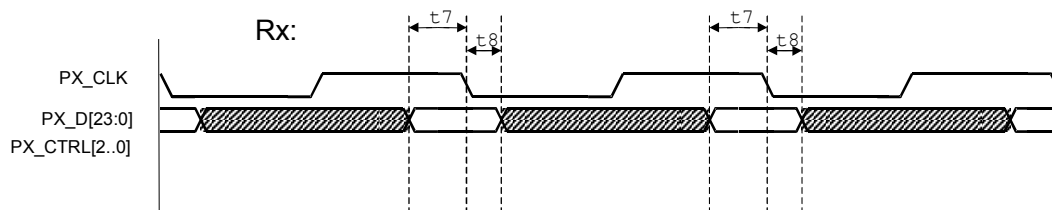


Figure 11: Rx Pixel interface timing diagram at falling edge

5.1.5 Side band interface timings

5.1.5.1 Rx Sideband Interface:

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Sideband data setup time to side band clock at Rx (500 MBit/s mode)	-	13	-	ns
t_2	Sideband data hold time to side band clock at Rx (500 MBit/s mode)	-	114	-	ns
t_1	Sideband data setup time to side band clock at Rx (1 GBit/s mode)	-	6,5	-	ns
t_2	Sideband data hold time to side band clock at Rx (1 GBit/s mode)	-	57	-	ns

Table 12: Sideband Timing Table at Rx Sideband Interface

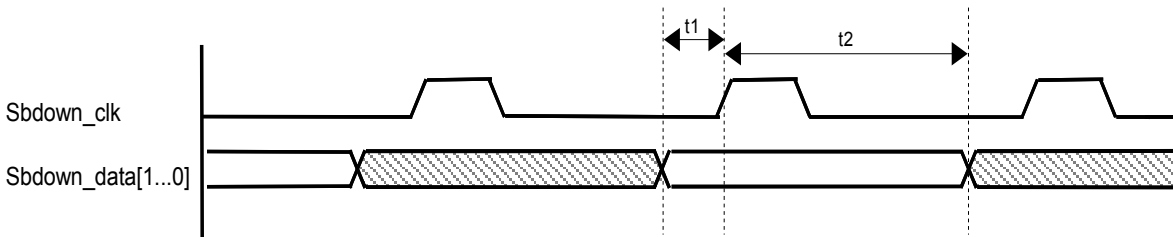


Figure 12: Rx Sideband interface timing diagram

5.1.5.2 Tx Sideband Interface

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Sideband data setup time to sideband clock at Tx	-	60	-	ns
t_2	Sideband data hold time to sideband clock at Tx	-	60	-	ns

Table 13: Sideband Timing Table at Tx Sideband Interface at 20.83 MHz serial upstream clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Sideband data setup time to sideband clock at Tx	-	40	-	ns
t_2	Sideband data hold time to sideband clock at Tx	-	40	-	ns

Table 14: Sideband Timing Table at Tx Sideband Interface at 31.25 MHz serial upstream clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Sideband data setup time to sideband clock at Tx	-	30	-	ns
t_2	Sideband data hold time to sideband clock at Tx	-	30	-	ns

Table 15: Sideband Timing Table at Tx Sideband Interface at 41.67 MHz serial upstream clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Sideband data setup time to sideband clock at Tx	-	20	-	ns
t_2	Sideband data hold time to sideband clock at Tx	-	20	-	ns

Table 16: Sideband Timing Table at Tx Sideband Interface at 62,5 MHz serial upstream clock

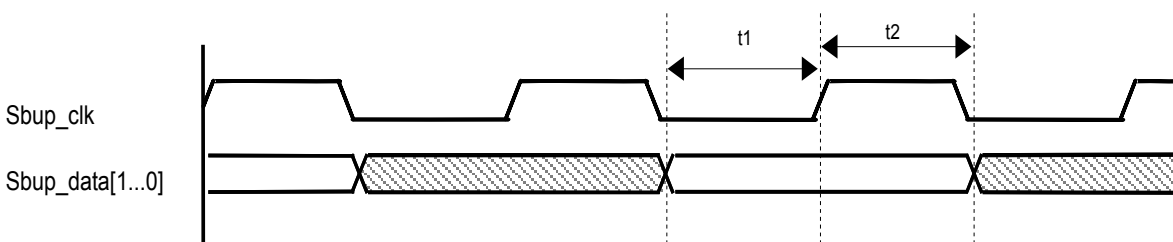


Figure 13: Tx Sideband interface timing diagram

5.1.6 configuration timings

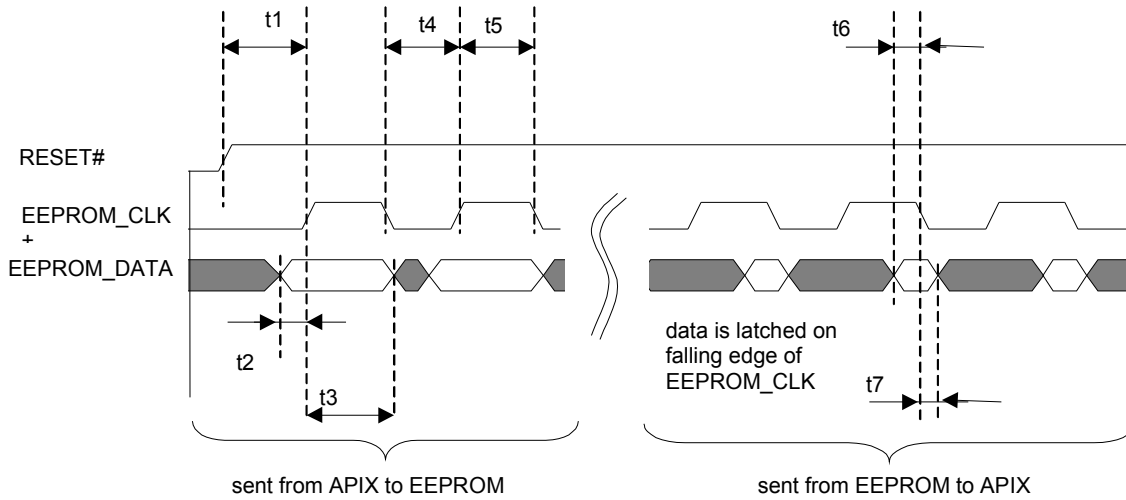


Figure 14: Timing diagram configuration

Parameter	Description	Min.	Typ.	Max	Unit
t_1	RESET high to first EEPROM clk	-	650	-	ns
t_2	setup time EEPROM_DATA to EEPROM_CLK	-	400	-	ns
t_3	hold time EEPROM_DATA to EEPROM_CLK	-	1200	-	ns
t_4	EEPROM_CLK low time	-	800	-	ns
t_5	EEPROM_CLK high time	-	800	-	ns
t_6	setup time EEPROM_DATA to EEPROM_CLK	-	20	-	ns
t_7	hold time EEPROM_DATA to EEPROM_CLK	-	10	-	ns

Table 17: timing diagram configuration

5.2 External Circuits

5.2.1 External Termination Resistors

Note: There are **NO** external termination resistors required – for both Upstream and Downstream the dedicated 50 Ω termination resistors are integrated in the circuit.

5.2.2 External Coupling Capacitors

5.2.2.1 Downstream Coupling Capacitors

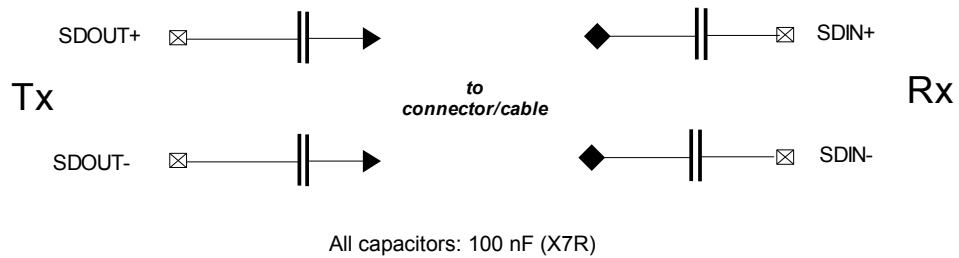


Figure 15: External Coupling capacitors in Downstream

5.2.2.2 Upstream Coupling Capacitors

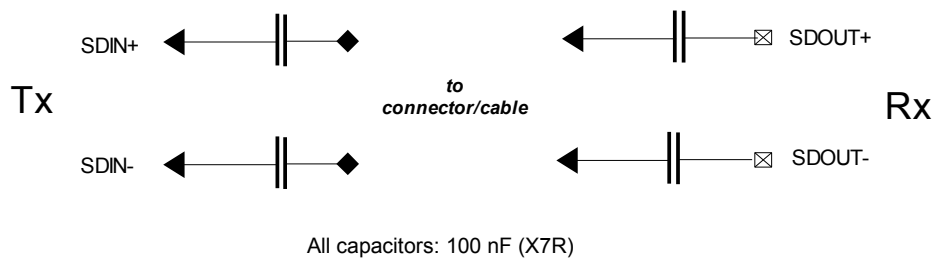


Figure 16: External Coupling capacitors in Upstream

5.2.3 External Loop Filter Specification

The APIX PLL circuits require an external RC loop filter. Figure 14 shows the external loop filter circuit for the core VCO. Figure 15 shows the circuit for the pixel clock VCO.

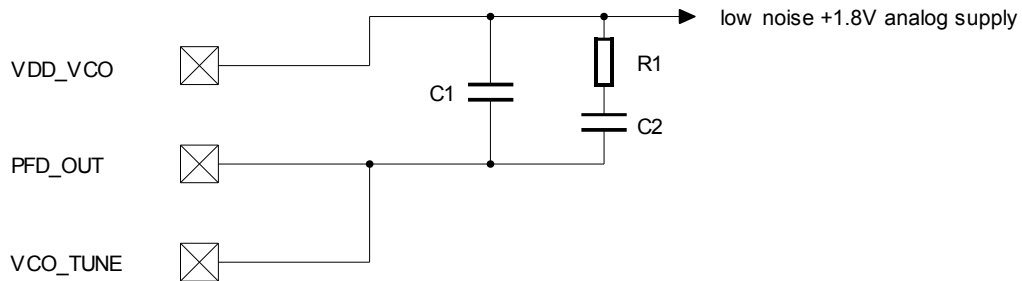


Figure 17: External loop filter circuit for system clk VCO

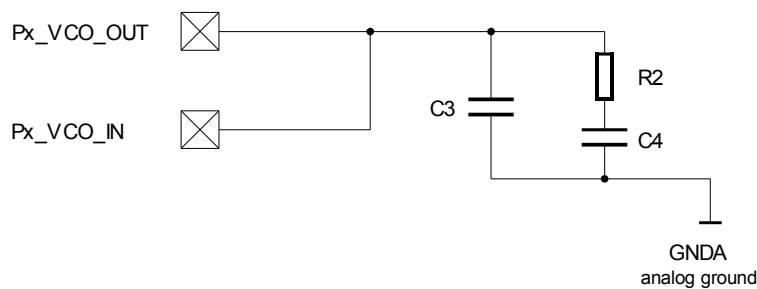


Figure 18: External loop filter circuit for pixel clock VCO at Rx

Table 13 shows the component values for the system clock VCO loop filter and for the pixel clock VCO loop filter. The use of SMD ceramic chip capacitors and chip resistors is recommended.

VCO	Signals	Parameter	Symbol	Value Tx	Value Rx	Units
core VCO	VDD_VCO	Loop Filter Capacitor C ₁	C ₁	1,5	10	nF
	PFD_OUT	Loop Filter Capacitor C ₂	C ₂	10	10	nF
	VCO_TUNE	Loop Filter Resistor R ₁	R ₁	220	100	kΩ
px clk VCO	Px_VCO_OUT	Loop Filter Capacitor C ₃	C ₃	-	2,2	nF
	Px_VCO_IN	Loop Filter Capacitor C ₄	C ₄	-	47	nF
		Loop Filter Resistor R ₂	R ₂	-	1	kΩ

Table 18: Loop filter values for system clk VCO and pixel clk VCO

5.2.4 External Reference Clock Circuit

The APIX core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal (Figure 19). Alternatively a stable 10 MHz clock signal (3.3 V CMOS TTL) can directly be connected to XTAL_IN with XTAL_OUT left open.

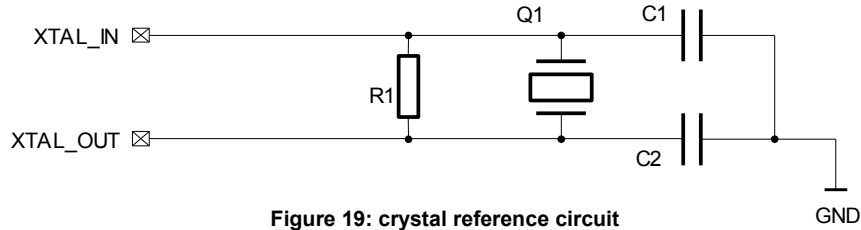


Figure 19: crystal reference circuit

Reference Clock Source	Signals	Parameter	Symbol	Value Tx	Value Rx	Units
clock crystal	XTAL_IN XTAL_OUT	clock frequency	Q ₁	10	10	MHz
		resistor	R ₁	2	2	MΩ
		capacitor	C ₁	33	33	pF
			C ₂	33	33	pF
3.3 V TTL oscillator	XTAL_IN	3.3 V TTL clock signal	-	10	10	MHz
	XTAL_OUT	unconnected	-	-	-	-

Table 19: Values for reference clock circuitry

Note: for proper link operation it is mandatory to use the same reference clock frequency at Tx and Rx side.

5.2.5 Reference Circuit of the Nominal and Pre-Emphasis Current (Tx)

For optimized signal integrity and lowest EMI in dependence of the quality and length of the STP cable used, the output nominal current and the pre-emphasis current of the APIX Tx device can be set individually by means of external resistors.

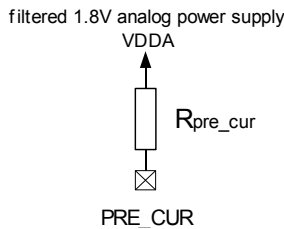


Figure 8: Pre-emphasis current

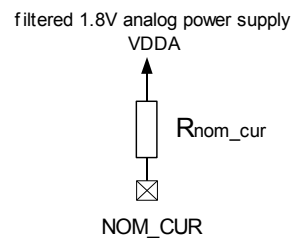


Figure 9: Nominal current

Resistor	Pin	recommended min/max values		
		resistor value (Ω)	min	max
R _{nom_cur}	NOM_CUR	resistor value (Ω)	min 500	max 10000
		typ. output current (mA)	max 5	min 0.5
R _{pre_cur}	PRE_CUR	resistor value (Ω)	min 500	max 10000
		typ. add-on output current (mA)	max 1	min 0.05

Table 20: Component values for nominal and pre-emphasis current

5.2.6 Reference Circuit of the Swing Control (Rx)

To achieve optimum transmission of the upstream link, the signal swing of the Rx device can be adjusted by means of an external resistor. When using the embedded upstream channel, the resistor controls the swing amplitude. When using the external upstream link, the resistor adjusts the nominal drive current.

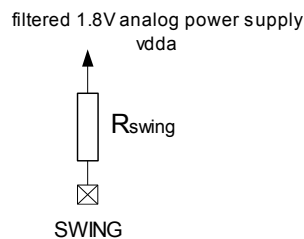


Figure 20: Rx nominal current

Pin	R _{swing}		Units
	min	max	
SWING	500	10000	Ω

Table 21: Component value for Rx nominal current / swing

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors is not liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V _{CC}	3.0.	3.6	V	
Input Voltage	V _{IN}	1.62	1.98	V	
I/O Current (DC or transient any pin)	I _D	-20	+20	mA	
Storage Temperature	T _{stg}	-55	+150	° C	
Max Soldering Temperature	T _{SLD} / T _{SLD}		260	° C	40 seconds maximum
ESD Voltage (CML I/Os vs. common GND & Supply)	V _{ESDCMLHBM}		t.b.d. ¹⁾	V	Human Body Model (HBM)
ESD Voltage (all other pin combinations)	V _{ESDOTHERHBM}		t.b.d. ¹⁾	V	Human Body Model (HBM)
ESD Voltage	V _{ESDCDM}		750	V	Charge Device Model (CDM)

Note: ¹⁾ Under qualification. For further information contact INOVA Semiconductors

Table 22: Absolute maximum ratings

6.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage Core / Analog VDD / VDDA	V _{CC CORE}	1.71	1.89	V	1.8 V ± 5%
DC Supply Voltage IO DVDD	V _{CC IO}	2.97	3.63	V	3.3 V ± 10%
CML Current	I _{CML}	0.8	24	mA	Internal Current Source
Ambient Temperature	T _a	-40	+105	° C	

Table 23: Recommended operating conditions

6.3 DC Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CMOS Input High Voltage	V _{IH}	V _{CC} = 3.3 V	2.0		V _{CC IO}	V
CMOS Input Low Voltage	V _{IL}	V _{CC} = 3.3 V	0		0.8	V
CMOS Input High Current	I _{IH}	V _{IN} = V _{CC}	-10		10	µA
CMOS Input Low Current	I _{IL}	V _{IN} = 0 V	-15		-77	µA
CMOS Output High Voltage	V _{OH}	I _{OH} = -4 mA	2.4			V
CMOS Output Low Voltage	V _{OL}	I _{OL} = 4 mA			0.4	V
CMOS Output High Current	I _{OH}	V _{OH} = 0.9 x V _{CC}			4	mA
CMOS Output Low Current	I _{OL}	V _{OL} = 0.1 x V _{CC}			-4	mA
Power Dissipation Tx	P _{max Tx}	max data transmission rate		170		mW
Power Dissipation Rx	P _{max Rx}	max data transmission rate		180		mW

Note: Floating CMOS inputs can result in excessive supply current. Therefore, unused inputs should be tied to V_{CC} or GND

Table 24: DC characteristics

6.3.1 Typical Supply Current

Parameter	Mode	Tx	Rx	Unit	Note
I _{vdd/vdd_osc} (1.8V digital core)	all	11	10	mA	
I _{vdda/vdd_vcc} (1.8V analog)	1 GBit/s	82	71	mA	Pattern: 000000/FFFFFF; max serial drive currents
I _{dvdd/dvdd_osc} (3.3V io)	10 bit / 6 MHz	7	6	mA	Rx Output Load: 12 pF
	10 bit / 62 MHz	7	6	mA	Rx Output Load: 12 pF
	24 bit / 6 MHz	7	6	mA	Rx Output Load: 12 pF
	24 bit / 32 MHz	7	6	mA	Rx Output Load: 12 pF

Table 25: DC characteristics

6.4 AC-Characteristics

Parameter	Min.	Typ.	Max.	Units
Input Capacitance, any pin		3	5	pF
Serial Transmission Gross Data Rate (Downstream)	500	-	1000	MBit/s
Serial Transmission Gross Data Rate (Upstream)	20.8	-	62.5	MBit/s
CMOS Output Rise / Fall Time (C _L = 10 pF)		5	10	ns

Table 26: AC characteristics

6.5 Reference Clock Specification

(T_a = -40 to +105°C; VDD/VDDA = 1.71 – 1.89 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Nominal Frequency	f _{osc}		10		MHz	
Frequency Jitter	F _{TOL}	-100		+100	ppm	

Table 27: Reference clock specification

6.6 Pixel Clock Range Specification Rx

(T_a = -40 to +105°C; VDD/VDDA = 1.71 – 1.89 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Pixel Clock Frequency	f _{PIX}	6		62,5	MHz	Maximum frequency depends on selected bit width

Table 28: Pixel Clock Range Specification

7 Package Options / Ordering Codes / Soldering Information

7.1 Package Options / Ordering Codes / Product Availability

To reduce pin count and save board space, the APIX devices are available in different QFN packages. All packages are fully RoHS-compliant.

Device / Ordering Code	Description	Package	Minimum order Quantity
Transmitter			
INAP125T12	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	416 pcs/tray
INAP125T12-R2	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	2000 pcs/reel
INAP125T12-R4	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	4000 pcs/reel
INAP125T24	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	260 pcs/tray
INAP125T24-R2	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	2000 pcs/reel
INAP125T24-R4	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	4000 pcs/reel
Receiver			
INAP125R12	Rx w/10...12 bit Interface + 1 bit Sideband	QFN52	260 pcs/tray
INAP125R12-R2	Rx w/10...12 bit Interface + 1 bit Sideband	QFN52	2000 pcs/reel
INAP125R12-R4	Rx w/10...12 bit Interface + 1 bit Sideband	QFN52	4000 pcs/reel
INAP125R24	Rx w/10...24 bit Interface + 2 bit Sideband	QFN64	260 pcs/tray
INAP125R24-R2	Rx w/10...24 bit Interface + 2 bit Sideband	QFN64	2000 pcs/reel
INAP125R24-R4	Rx w/10...24 bit Interface + 2 bit Sideband	QFN64	4000 pcs/reel

Note: Engineering Samples suffix: XS / under AEC-Q100 qualification

For detailed **Tray** or **Tape & Reel Specification** please contact INOVA Semiconductors

7.2 Soldering Information

The detailed **Soldering Profile** can be obtained from INOVA Semiconductors' web page.

Note: The **exposed die attach pad** (see package drawings chapter 8.3) of the QFN package provides excellent thermal dissipation, high frequency benefits and mechanical stability. It is mandatory to soldering the copper die attach pad directly onto the PCB's ground.

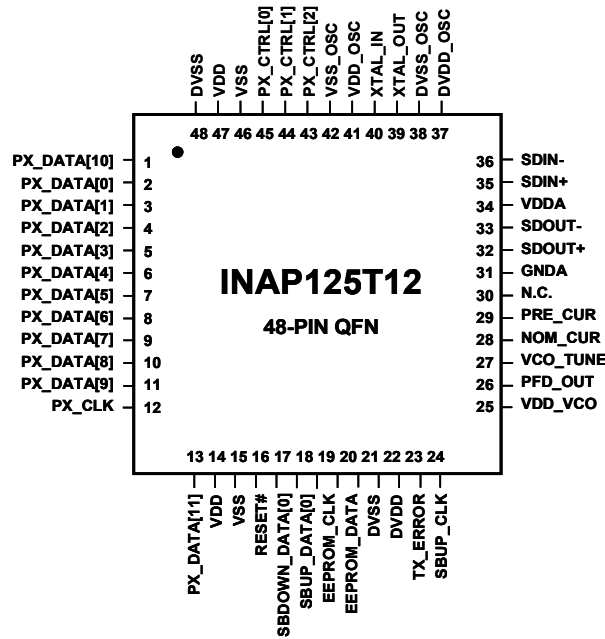
7.3 RoHS compliance

The devices INAP125R12, INAP125T12, INAP125R24 and INAP125T24 are released as RoHS compliant.

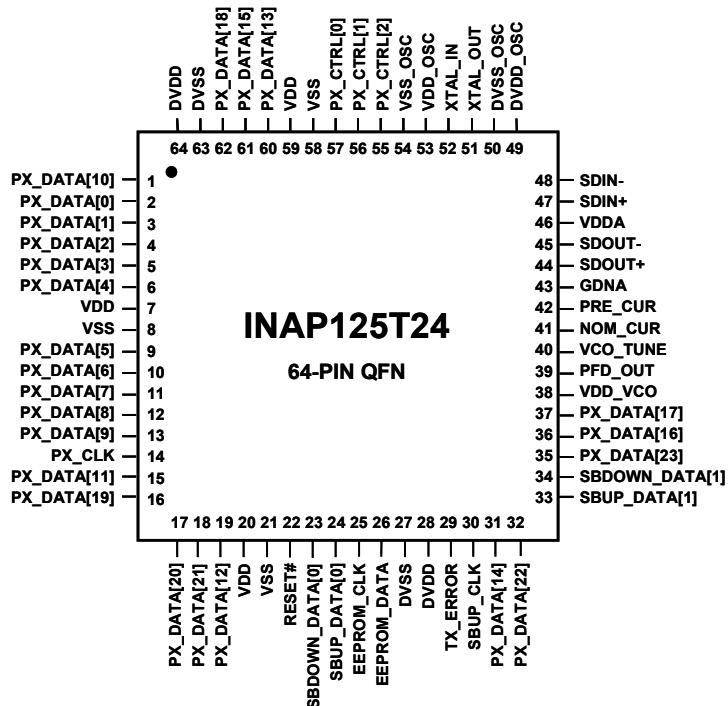
8 Pinouts / Package Dimensions

8.1 Pinouts

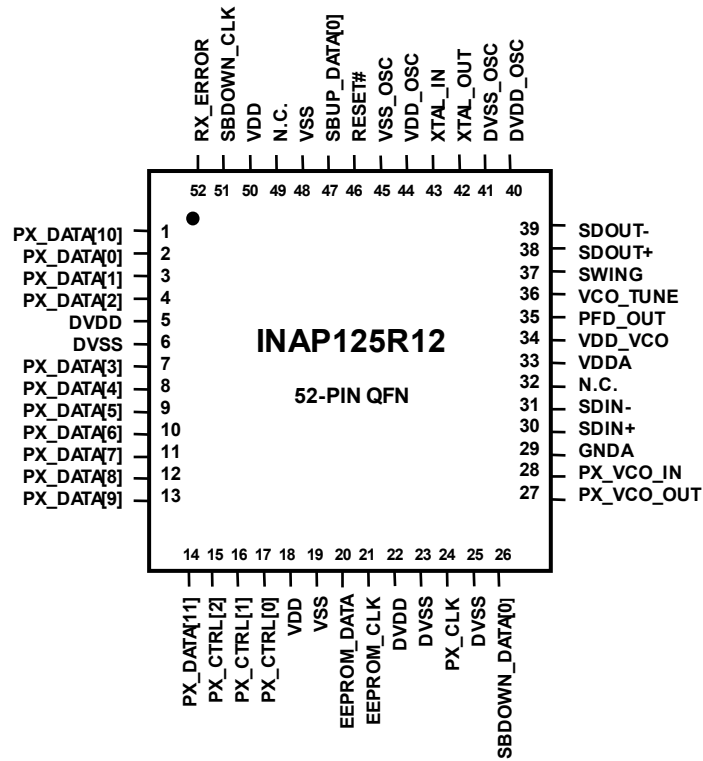
8.1.1 APIX Transmitter INAP125T12



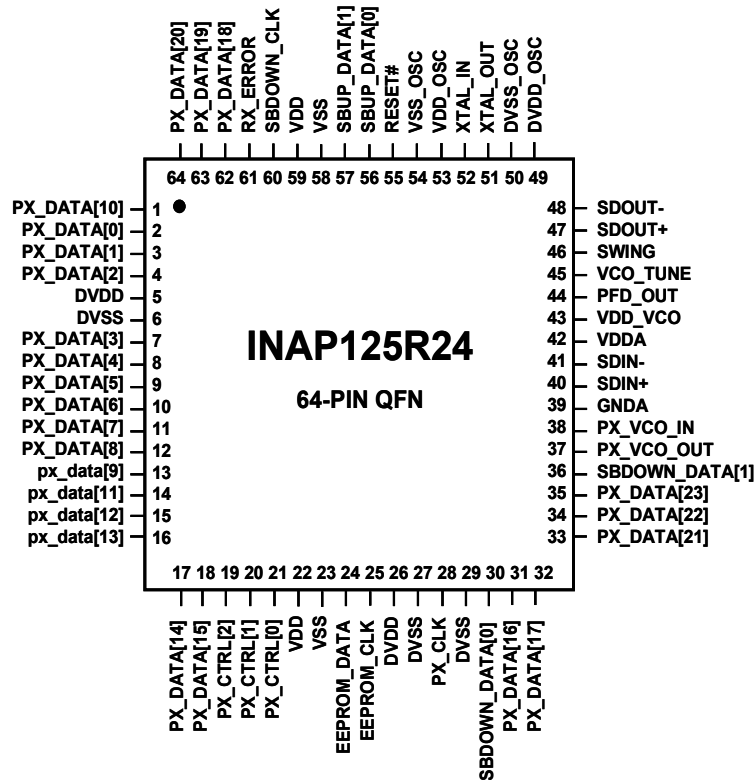
8.1.2 APIX Transmitter INAP125T24



8.1.3 APIX Receiver INAP125R12

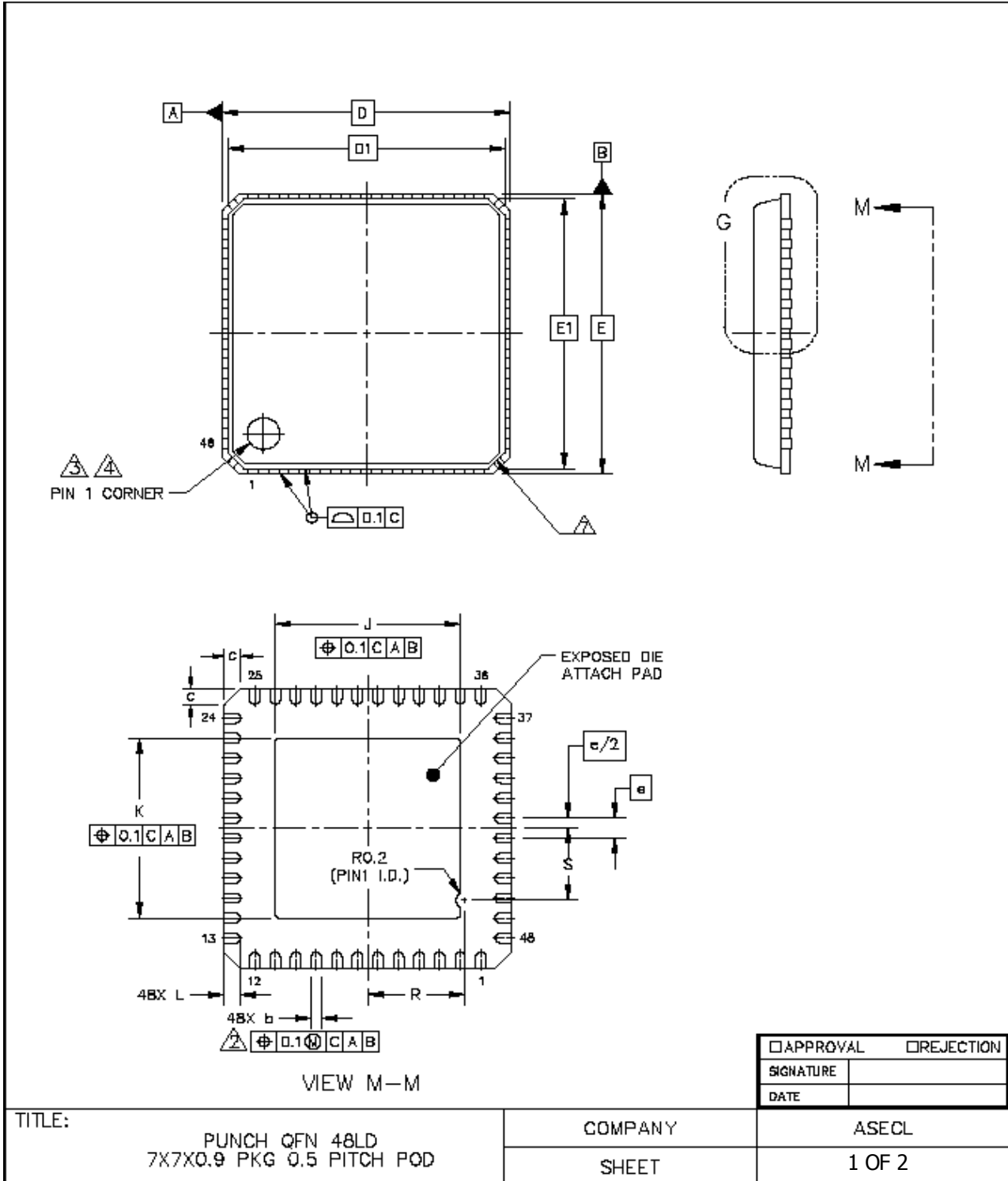


8.1.4 APIX Receiver INAP125R24

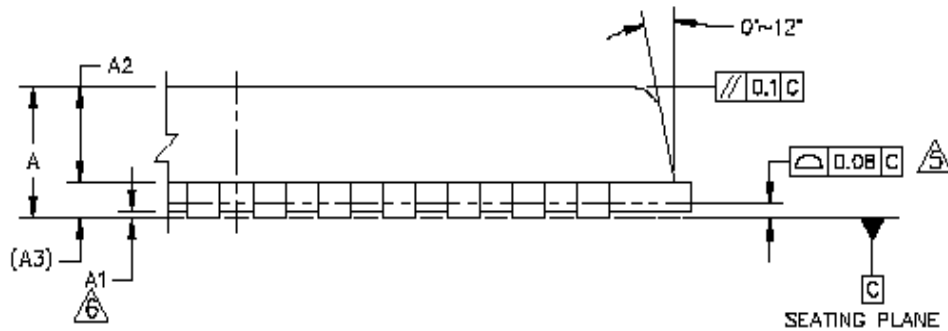


8.2 Package Dimensions (all values in mm)

48-PIN QFN



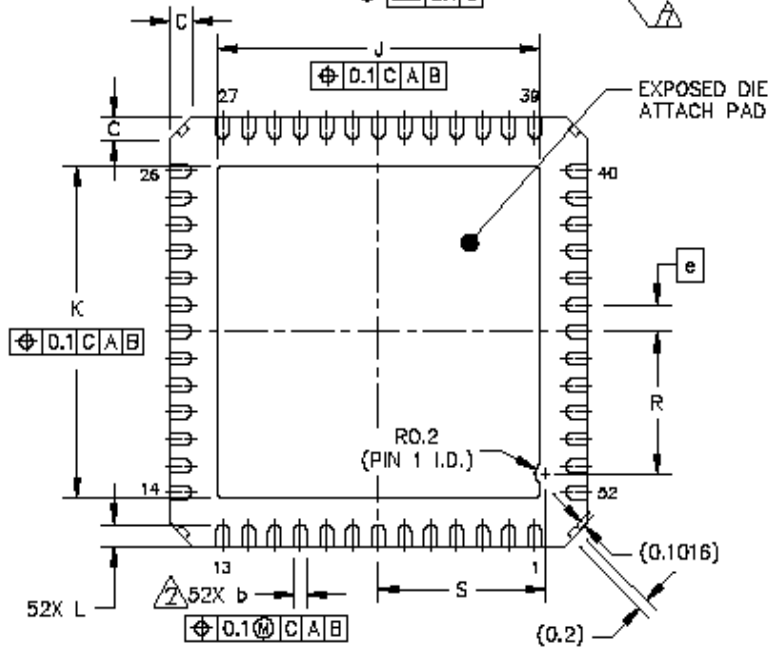
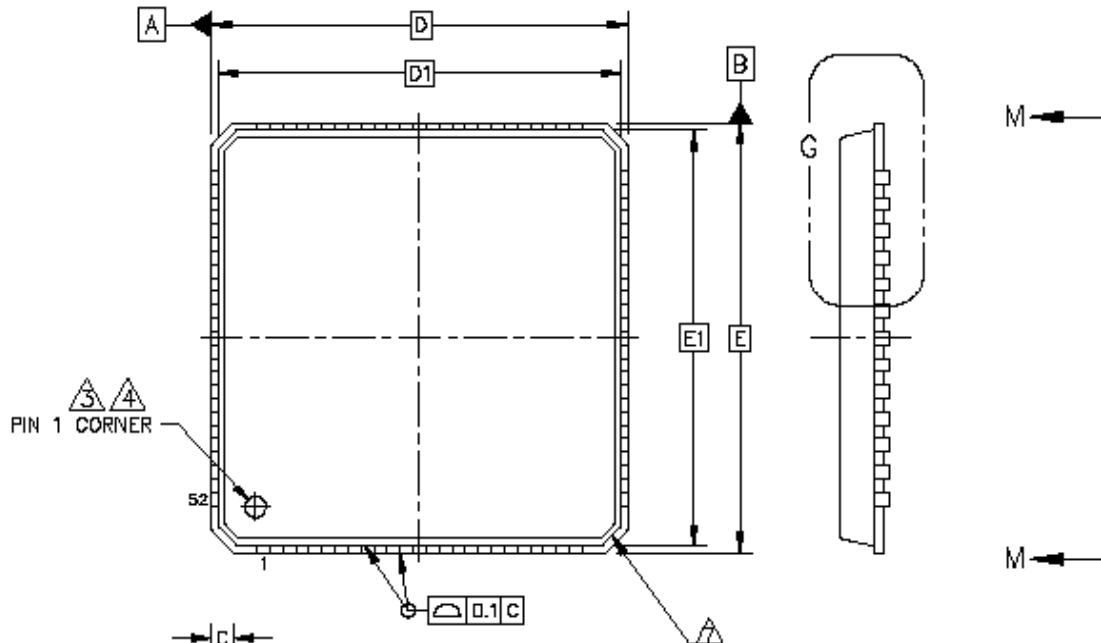
48-PIN QFN (cont'd)



DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX	NOTES		
A	0.8		0.9	1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM) ⚠ DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP. ⚠ THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. ⚠ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL. ⚠ APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING. ⚠ APPLIED ONLY TO TERMINALS. ⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.		
A1	0	0.02	0.05			
A2	0.65		0.69			
A3	0.203 REF.					
b	0.18	0.25	0.3			
C	0.24	0.42	0.6			
D	7 BSC					
D1	6.75 BSC					
E	7 BSC					
E1	6.75 BSC					
e	0.5 BSC					
J	4.4	4.5	4.6			
K	4.4	4.5	4.6			
L	0.3	0.4	0.5			
R	2.25	2.35	2.45			
S	1.7	1.8	1.9			
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52-PIN QFN



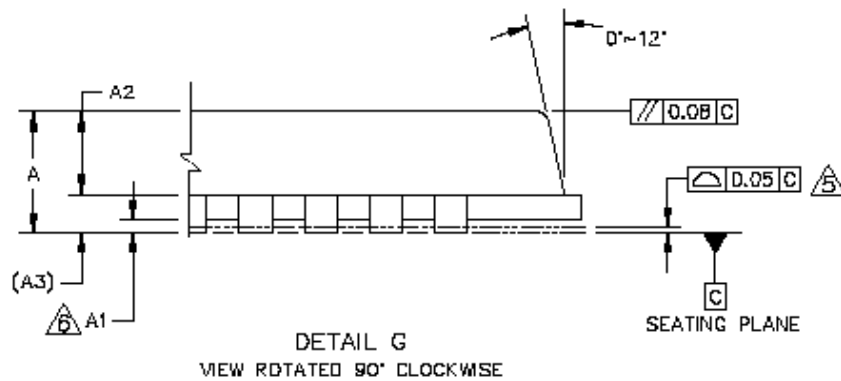
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DATE	

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8X8X0.9 PKG 0.5 PITCH POD

COMPANY
SHEET

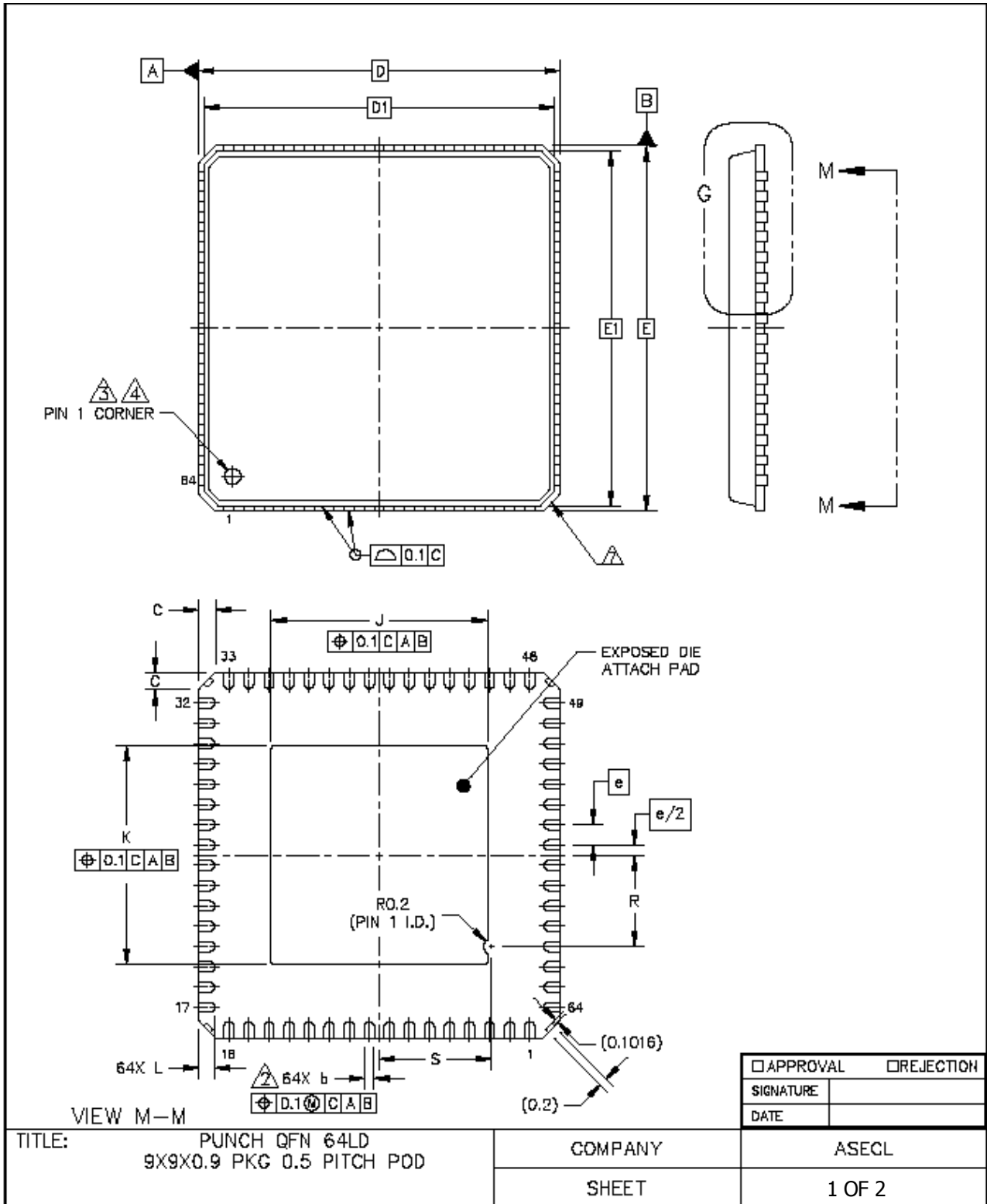
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1 OF 2

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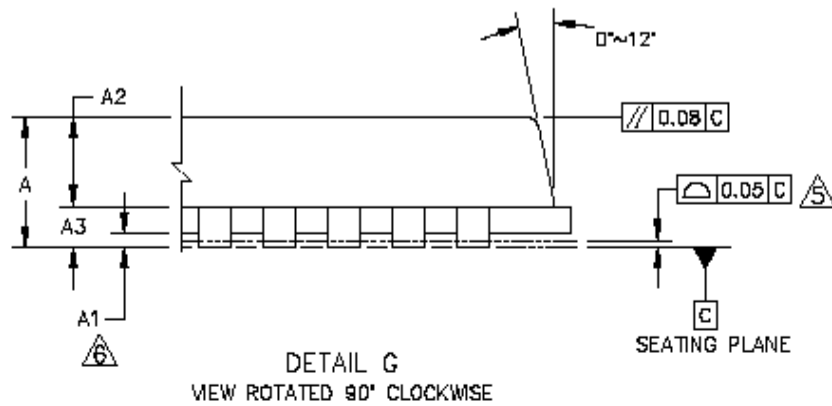


DIM	MIN	NOM	MAX	NOTES		
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A1	0	0.02	0.05			
A2	0.65		0.69			
A3		0.203 REF				
b	0.18	0.25	0.3			
C	0.24	0.42	0.6			
D		8 BSC				
D1		7.75 BSC				
E		8 BSC				
E1		7.75 BSC				
e		0.5 BSC				
J	6.1	6.2	6.3			
K	6.1	6.2	6.3			
L	0.3	0.4	0.5			
R	2.55	2.65	2.75			
S	3.1	3.2	3.3			
					UNIT	DIMENSION AND TOLERANCES
				UNIT	ASME_Y14.5M	---
TITLE:				COMPANY		ASECL
PUNCH QFN 52LD 8X8X0.9 PKG 0.5 PITCH POD				SHEET		2 OF 2

64-PIN QFN



64-PIN QFN (cont'd)




DIM	MIN	NOM	MAX	NOTES
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A1	0	0.02	0.05	
A2	0.65		0.69	
A3		0.203 REF		
b	0.18	0.25	0.3	
C	0.24	0.42	0.6	
D		9 BSC		
D1		8.75 BSC		
E		9 BSC		
E1		8.75 BSC		
e		0.5 BSC		
J	5.3	5.4	5.5	
K	5.3	5.4	5.5	
L	0.3	0.4	0.5	
R	2.15	2.25	2.35	
S	2.7	2.8	2.9	
				UNIT
				DIMENSION AND TOLERANCES
				REFERENCE DOCUMENT
				UNIT
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TITLE: PUNCH QFN 64LD 9X9X0.9 PKG 0.5 PITCH POD				COMPANY
				ASEGL
				SHEET
				2 OF 2

9 Revision History

- V 1.0 Released Data Sheet
-

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