



AL460
Full HD FIFO Memory
Datasheet

Preliminary Version 0.02

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Amendments

Revise Date	Contents	Page
08.07.01	Preliminary version 0.01	
08.07.03	Add Mechanical Drawing	27
08.07.21	Remove UXGA Graphic data support	4, 5
08.07.23	<ul style="list-style-type: none"> ▪ Revise PIN DIAGRAM & PIN DEFINITION ▪ Add FUNCTION BLOCK DIAGRAM ▪ Revise "Power-On-Reset Operation" (Sec 8.1) description ▪ Add RSTN timing diagram ▪ Add "Two Frame Mode" description and Timing diagrams ▪ Add "External Decoupling Circuit" reference schematic 	
08.07.30	Change part number to AL460	
08.08.07	<ul style="list-style-type: none"> ▪ Revise WFSEL, RFSEL, RCLKO, RSTN and TFEN pins description ▪ Change PIN DIAGRAM Marking ▪ Add "Standard FIFO Mode" & "Two Frame Mode" DIAGRAM ▪ Add Electrical Characteristics parameters 	

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1 GENERAL DESCRIPTION

The AL460 consists of 128Mbit of memory density and can be configured as 8M x 16-bits FIFO (first in first out) at maximum R/W operating speed 150MHz. The full HD FIFO can be used in a wide range of applications such as Multimedia, video capture systems and many other varieties of video data buffering applications. The size and high-speed data access allow full HD video frame capture up to 1080p resolutions.

The AverLogic AL460 FIFO memory provides completely independent input and output ports. The built-in address and pointer control circuits provide a straightforward bus interface to sequentially read/write memory that can reduce inter-chip design efforts.

The AL460 uses high performance process technologies with extended controller functions (write mask, read skip .. etc.); allows easy operation of non-linearity FIFO read/write for use in broadcasting systems, security systems, camera and many other applications. An additional feature, dual chip cascading, is also available to double FIFO size.

The AL460 is designed and manufactured using state-of-the-art technologies with low power consumption AC characteristics (2.5 & 3.3V power supply) facilitating high performance and high quality applications.

The chip is available in LQFP-128 pin package; the small footprint allows product designers to keep board real estate to a minimum.

2 FEATURES

- 128Mbit density 8M x 16-bits configuration
- Supports video NTSC, PAL and HDTV up to 1080p resolution
- Independent 16-bit read/write operations (different I/O data rates acceptable) at maximum speeds 150Mhz
- High speed synchronous sequential access
- Input/Output enable control
- Polarity Selectable
- 2.5V & 3.3V power supply
- Standard 128-pin LQFP package

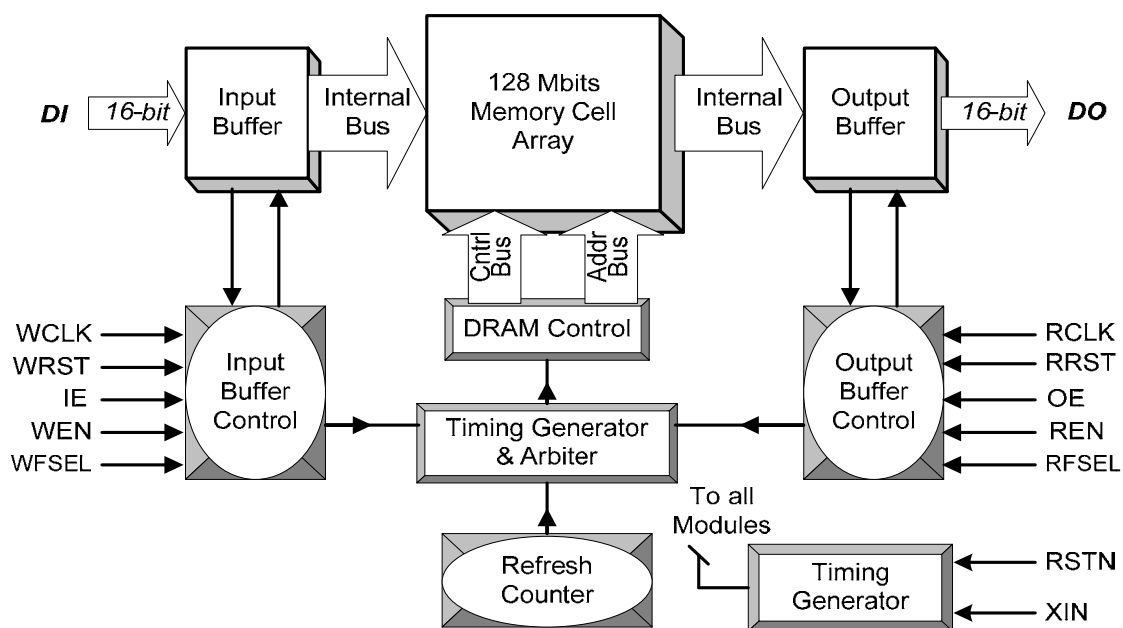
3 APPLICATIONS

- HD video capture and editing systems
- Switcher or format converter box
- Video capture or editing systems
- Video data buffering for security systems
- Scan rate converters
- TBC (Time Base Correction) systems
- Frame synchronizer
- Digital video camera

- Hard disk cache memory
- Buffer for communication systems
- 1080p video data stream buffering

4 FUNCTION BLOCK DIAGRAM

The internal structure of each AL460 consists of Input/Output buffers, Write Data Registers, Read Data Registers and main 8M x 16-bit memory cell array and the state-of-the-art logic design that takes care of addressing and controlling the read/write data.



AL460 Block Diagram

5 ORDERING INFORMATION

Part number	Package	Power Supply	Status
AL460A-PBF	LQFP-128	+2.5V & +3.3 V	2008

Note: AverLogic Technologies PB-free products employ special PB-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's PB-free products are MSL classified at PB-free peak reflow temperatures that meet or exceed the PB-free requirements of IPC/JEDEC J Std-020C."

6 PIN DIAGRAM

6.1 Pin Description

Write Bus Signals

Pin name	Pin number	I/O type	Description
DI[15:0]	58, 56~51, 49~46, 44~41, 39	I	16-bit data inputs; synchronized with the WCLK clock. Data is acquired at the rising edge of WCLK clock.
WEN	37	I	WEN is the write enable signal that controls the 16-bit input data write and write pointer operation
IE	36	I	IE is the data input enable signal that controls the enabling/ disabling of the 16-bit data input pins. The internal write address pointer is always incremented at rising edge of WCLK by enabling WEN regardless of the IE level.
WCLK	38	I	WCLK is the write clock input pin. The write data input is synchronized with this clock.
WRST	35	I	The WRST is the write rest signal that resets the write address pointer to 0.
WFSEL	34	I	Write Frame select pin in Two Frame Mode (TFEN = H): 0: Frame 0 1: Frame 1

*Note: For the polarity definition of all write control signals (WEN, IE and WRST), please refer to PLRTY pin definition and “Memory Operation” section for details.

Read Bus Signals

Pin name	Pin number	I/O type	Description
DO[15:0]	102, 104~107, 109~111, 113~115, 117~120, 122	O	16-bit data outputs; synchronized with the RCLK clock. Data is output at the rising edge of the RCLK clock.
REN	125	I	REN is the read enable signal that controls the 16-bit output data read and read pointer operation.
OE	126	I	OE is the data input enable signal that controls the enabling/ disabling of the 16-bit data output pins. The internal read address pointer is always incremented at rising edge of RCLK by enabling REN regardless of the OE level.
RCLK	124	I	RCLK is the read clock input pin. The read data output is synchronized with this clock.

RCLKO	123	O	RCLK loop out
RRST	127	I	The RRST is the read reset signal that resets the read address pointer to 0.
RFSEL	74	I	Read Frame select pin in Two Frame Mode (TFEN = H): 0: Frame 0 1: Frame 1

*Note: For the polarity definition of all read control signals (REN, OE and RRST), please refer to PLRTY pin definition and “Memory Operation” section for details.

Power/Ground Signals

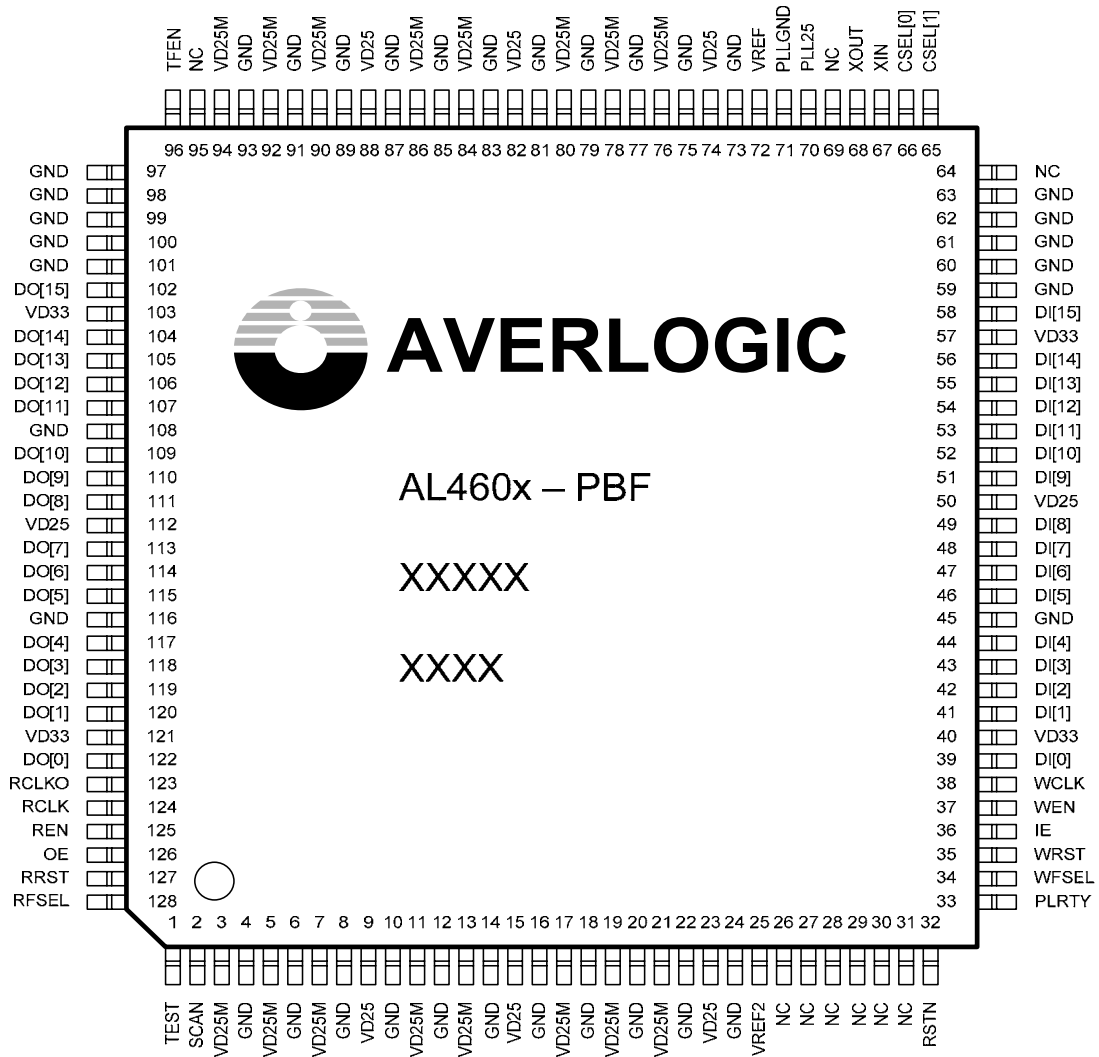
Pin name	Pin number	I/O type	Description
VD25M	3, 5, 7, 11, 13, 17, 19, 21, 76, 78, 80, 84, 86, 90, 92, 94	-	2.5V \pm 10% power supply for internal memory
VD25	9, 15, 23, 50, 74, 82, 88, 112	-	2.5V \pm 10% power supply for internal control logic
PLL25	70	-	2.5V \pm 10% power supply for internal PLL
PLLGND	71	-	PLL GND
VD33	40, 57, 103, 121	-	3.3V \pm 10% I/O power supply
GND	4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 45, 59~63, 73, 75, 77, 79, 81, 83, 85, 87, 89, 91, 93, 97~101, 108,		GND

Miscellaneous Signals

Pin name	Pin number	I/O type	Description
RSTN	32	I	Master reset (active Low)
PLRTY	33	I	Select active polarity of the control signals including WEN, REN, WRST, RRST, IE and OE totally 6 signals PLRTY = VD33, active low. PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VD33 or GND. If PLRTY level is changed during memory operation, memory data is not guaranteed.
XIN	67	I	Crystal input
XOUT	68	O	Crystal output
CSEL[1:0]	65, 66	I	Crystal input frequency select pins

			<ul style="list-style-type: none"> ▪ “00” - 11.059200MHz ▪ “01” - 20.000000MHz ▪ “10” - 24.576000MHz ▪ “11” - 14.318180MHz
VREF	72	AI	Reference voltage input * Please refer to “External decoupling circuit” application note for details
VREF2	25	AI	Reference voltage input 2 * Please refer to “External decoupling circuit” application note for details
TFEN	96	I	Two frame mode enable: <ul style="list-style-type: none"> ▪ “0” – Standard FIFO Mode ▪ “1” – Two Frame Mode
TEST	1	I	Test pin (pull-down for normal operation)
SCAN	2	I	Scan mode Enable (pull-down for normal operation)
NC	26~31, 64, 69, 95	-	No connect or connect to Ground

6.2 Pin Diagram



7. ELECTRICAL CHARACTERISTICS (TBC)

7.1 Absolute Maximum Ratings under Free-Air Temperature

(Excessive ratings are harmful to the lifetime. Only for user guidelines, not tested.)

Parameter		Rating	Unit
VD33	3.3V I/O Supply Voltage	-0.3 ~ +4.5	V
VD25M	2.5V Memory Voltage	-0.3 ~ +3.4	V
VD25	2.5V Core Voltage	-0.3 ~ +3.4	V
PLL25	2.5V PLL Voltage	-0.3 ~ +3.4	V
V _P	Pin Voltage	-0.3 ~ +(VD33 + 0.3)	V
I _O	Output Current	-20 ~ +20	mA
T _{AMB}	Ambient Op. Temperature	0 ~ +70	°C
T _{stg}	Storage temperature	-40 ~ +125	°C

7.2 Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD25M	2.5V Memory Voltage	2.25	2.5	2.75	V
VD25	2.5V Core Voltage	2.25	2.5	2.75	V
PLL25	2.5V PLL Voltage	2.25	2.5	2.75	V
V _{IH}	High Level Input Voltage	0.7VD33	-	VD33	V
V _{IL}	Low Level Input Voltage	0	-	0.3VD33	V

7.3 DC Characteristics

(V_{DD} = 3.3V, V_{SS} = 0V, T_{AMB} = 0 to 70°C)

Parameter		Min	Typ	Max	Unit
I _{CC}	Operating Current		TBD		mA

I_{SB}	Standby Current		TBD		mA
V_{OH}	Hi-level Output Voltage	VD33-0.4			V
V_{OL}	Lo-level Output Voltage			0.4	V
I_{LI}	Input Leakage Current (No pull-up or pull-down)	-10		+10	μ A
I_{LO}	Output Leakage Current (No pull-up or pull-down)	-10		+10	μ A
R_L	Input Pull-up/Pull-down Resistance		60		K Ω

7.4 AC Characteristics

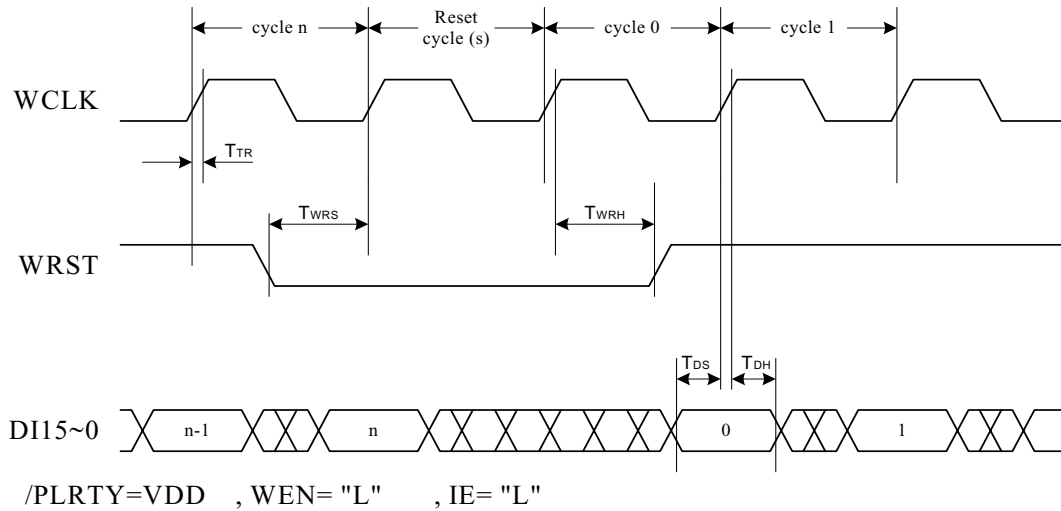
($V_{DD} = 3.3V$, $V_{SS} = 0V$, $T_{AMB} = 0$ to $70^{\circ}C$)

Parameter		150MHZ		Unit
		Min	Max	
T_{WC}	WCLK Cycle Time	6.6	-	ns
T_{WPH}	WCLK High Pulse Width	2.6	-	ns
T_{WPL}	WCLK Low Pulse Width	2.6	-	ns
T_{RC}	RCLK Cycle Time	6.6	-	ns
T_{RPH}	RCLK High Pulse Width	2.6	-	ns
T_{RPL}	RCLK Low Pulse Width	2.6	-	ns
T_{AC}	Access Time	3.0	8.0	ns
T_{OH}	Output Hold Time			ns
T_{HZ}	Output High-Z Setup Time			ns
T_{LZ}	Output Low-Z Setup Time			ns
T_{WRS}	WRST Setup Time	0.5	-	ns
T_{WRH}	WRST Hold Time	2.5	-	ns
T_{RRS}	RRST Setup Time	0.5	-	ns
T_{RRH}	RRST Hold Time	2.5	-	ns
T_{DS}	Input Data Setup Time	0.5	-	ns
T_{DH}	Input Data Hold Time	2.5	-	ns
T_{WES}	WEN Setup Time	0.5	-	ns
T_{WEH}	WEN Hold Time	2.5	-	ns
T_{WPW}	WEN Pulse Width	3.0	-	ns
T_{RES}	REN Setup Time	0.5	-	ns

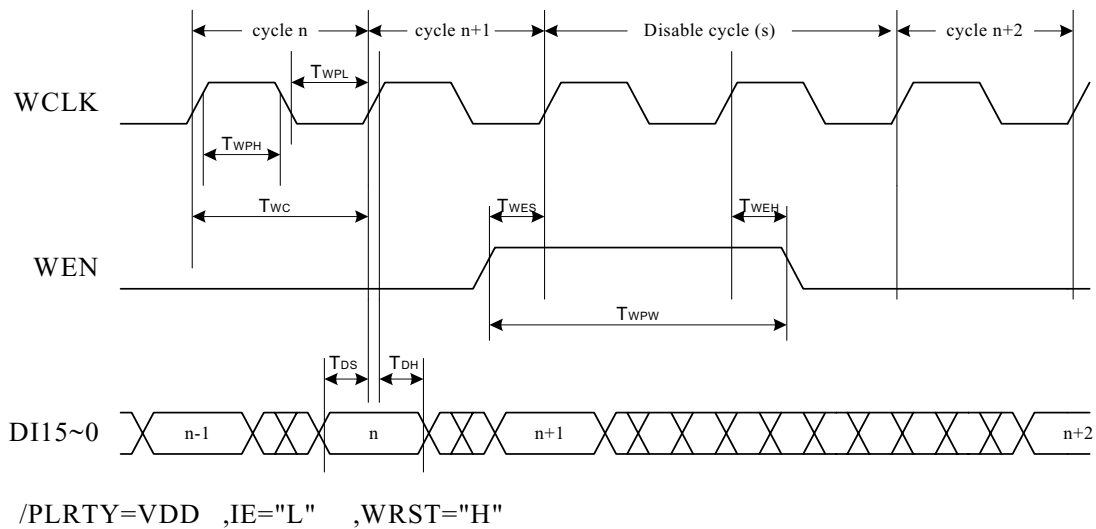
T_{REH}	REN Hold Time	2.5	-	ns
T_{RPW}	REN Pulse Width	3.0	-	ns
T_{IES}	IE Setup Time	0.5	-	ns
T_{IEH}	IE Hold Time	2.5	-	ns
T_{IPW}	IE Pulse Width	3.0	-	ns
T_{OES}	OE Setup Time	0.5	-	ns
T_{OEH}	OE Hold Time	2.5	-	ns
T_{OPW}	OE Pulse Width	3.0	-	ns
T_{TR}	Transition Time			ns
C_I	Input Capacitance			pF
C_O	Output Capacitance			pF

Note: The read address needs to be at least 1536 cycles after write address to guarantee new data read.

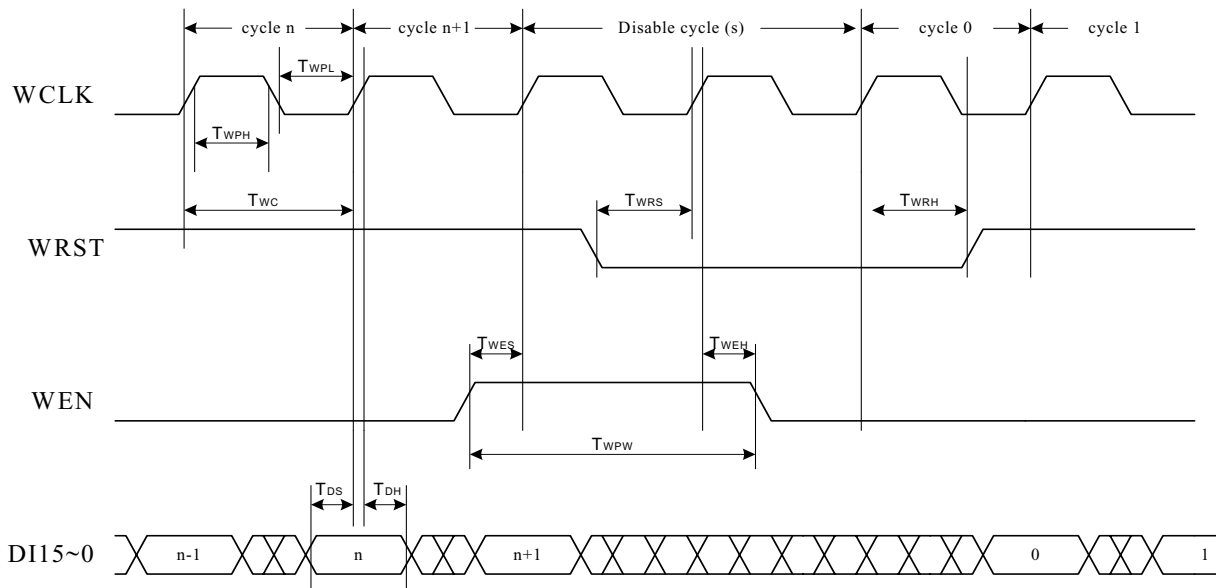
7.5 Timing Diagrams



Write Cycle Timing (Write Reset)

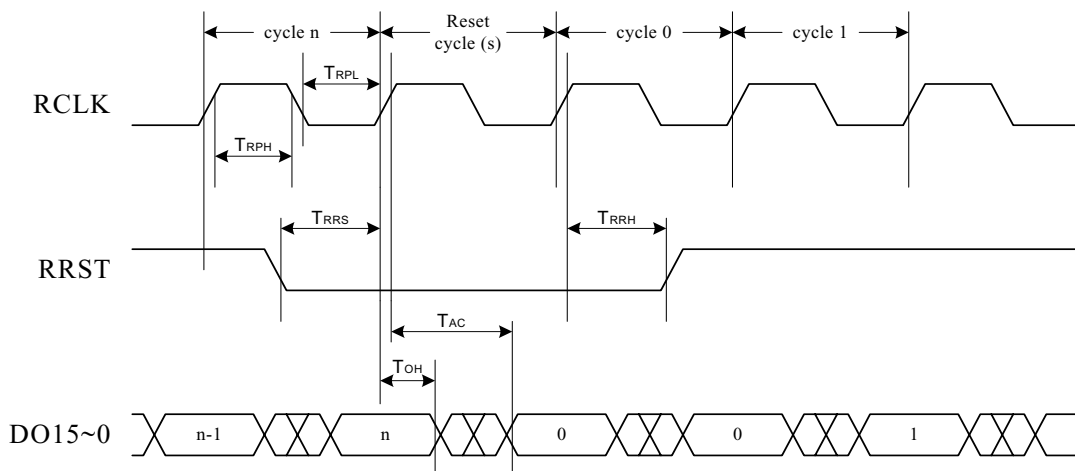


Write Cycle Timing (Write Enable)



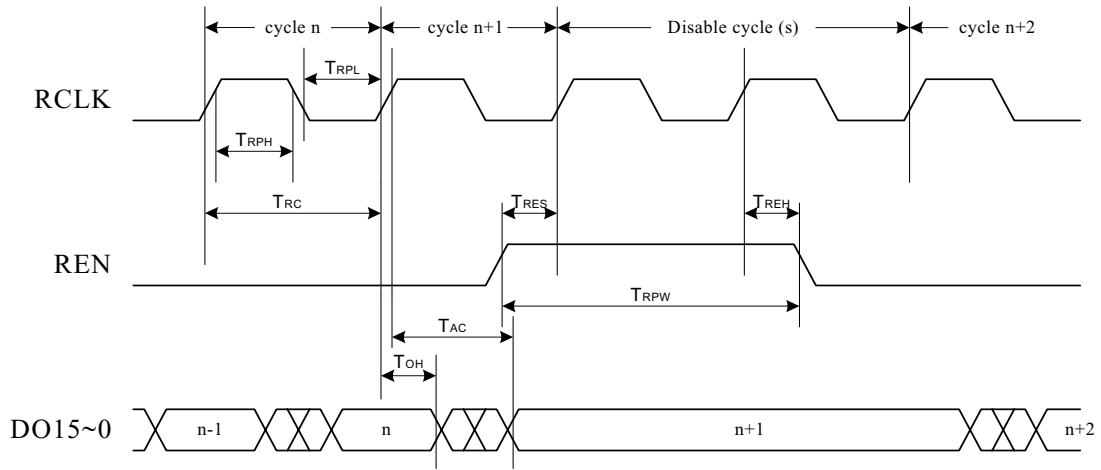
`/PLRTY=VDD ,IE="L"`

Write Cycle Timing (WEN, WRST)



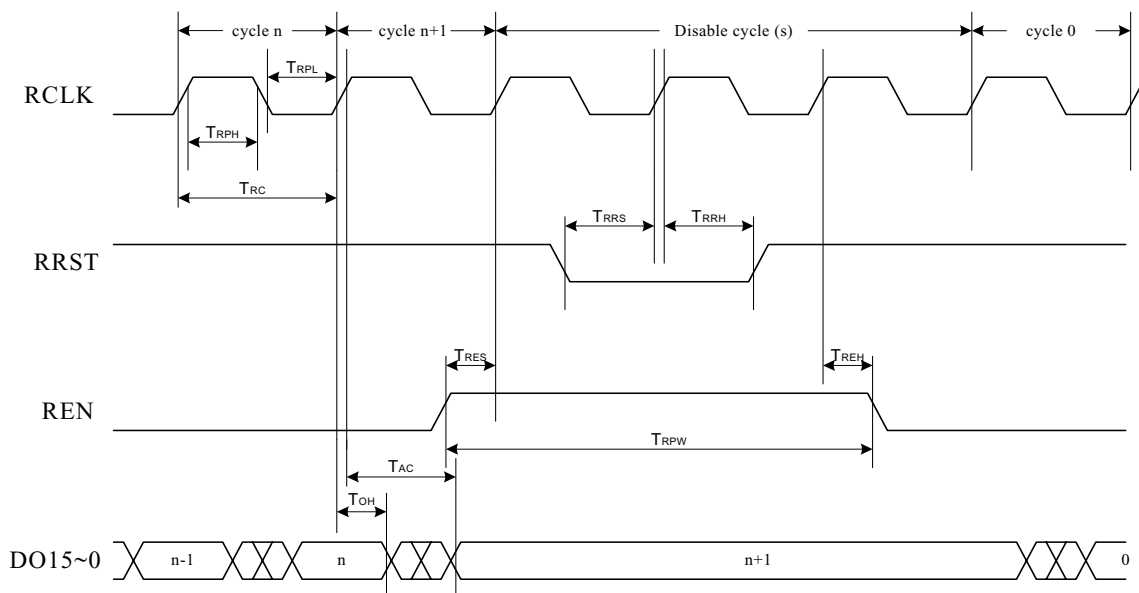
`/PLRTY=VDD ,REN="L" ,OE="L"`

Read Cycle Timing (Read Reset)



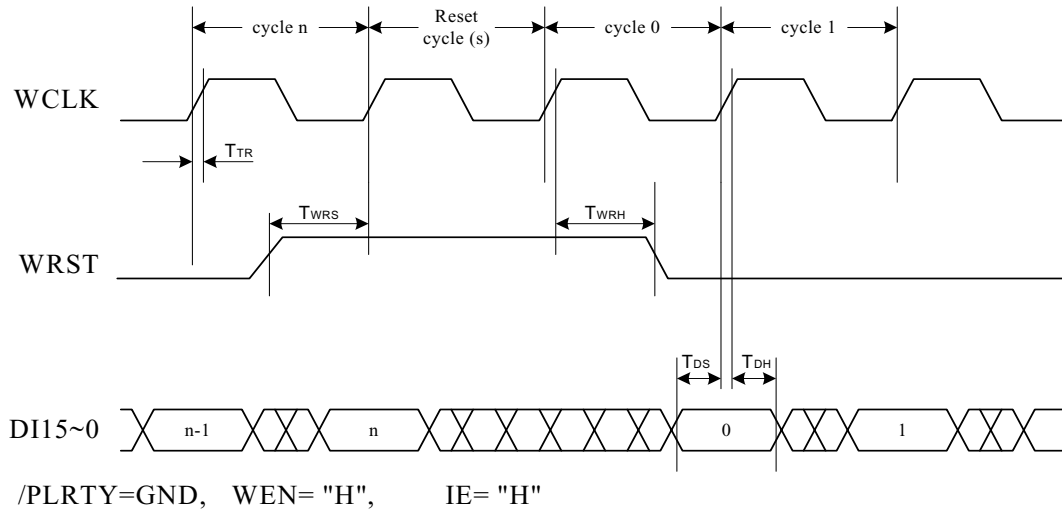
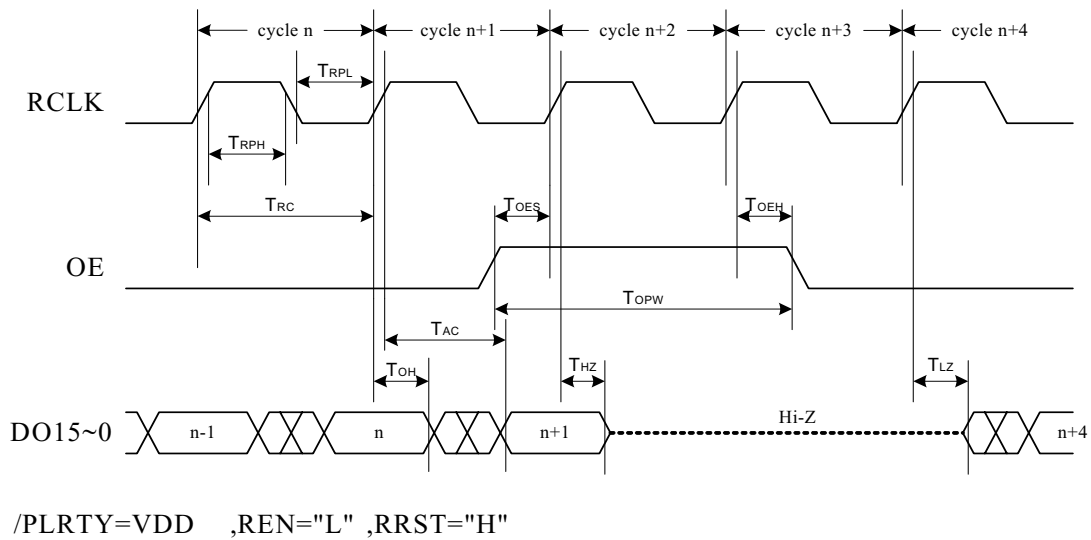
`/PLRTY=VDD ,OE="L" ,RRST="H"`

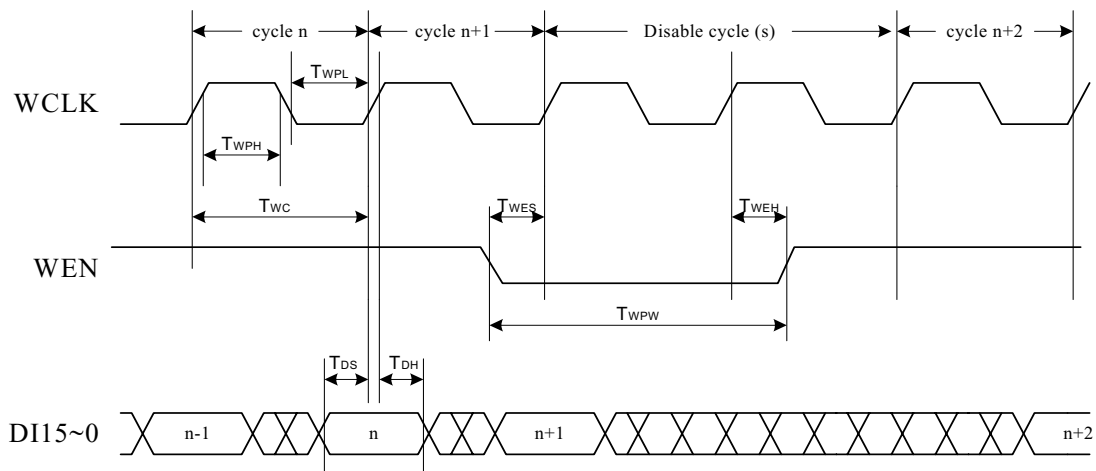
Read Cycle Timing (Read Enable)



`/PLRTY=VDD ,OE="L"`

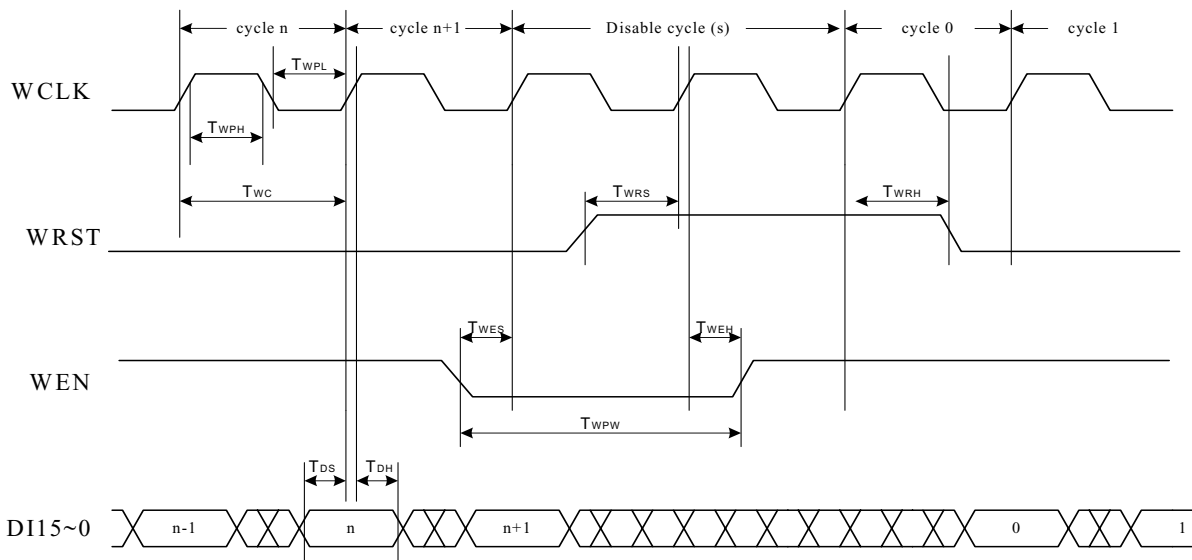
Read Cycle Timing (REN, RRST)


Write Cycle Timing (Write Reset)

Read Cycle Timing (Output Enable)



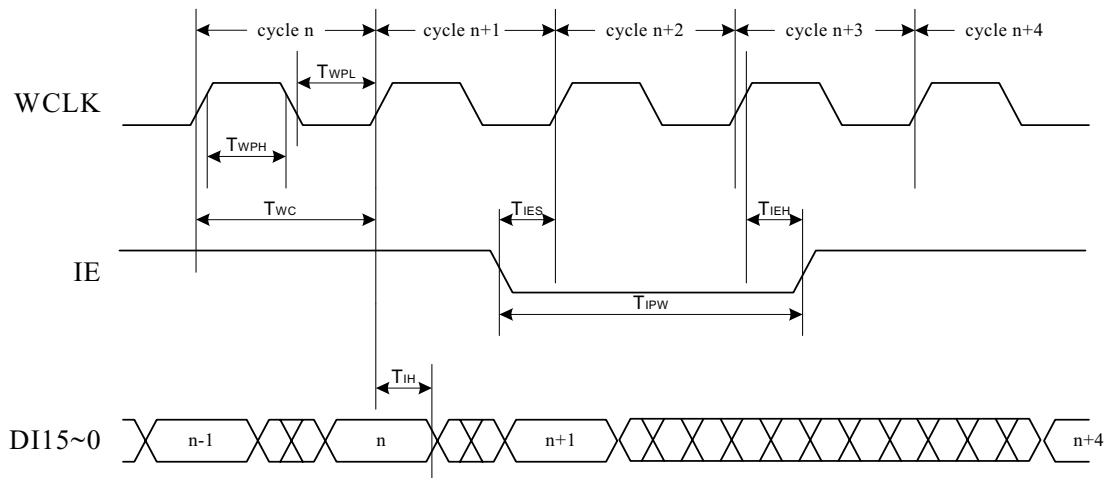
`/PLRTY=GND, IE="H", WRST="L"`

Write Cycle Timing (Write Enable)



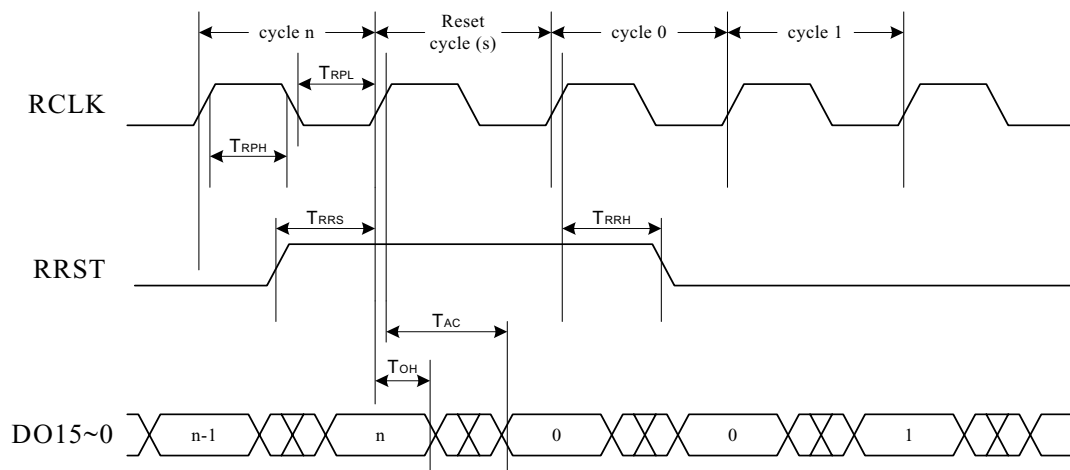
`/PLRTY=GND, IE="H"`

Write Cycle Timing (WE, WRST)



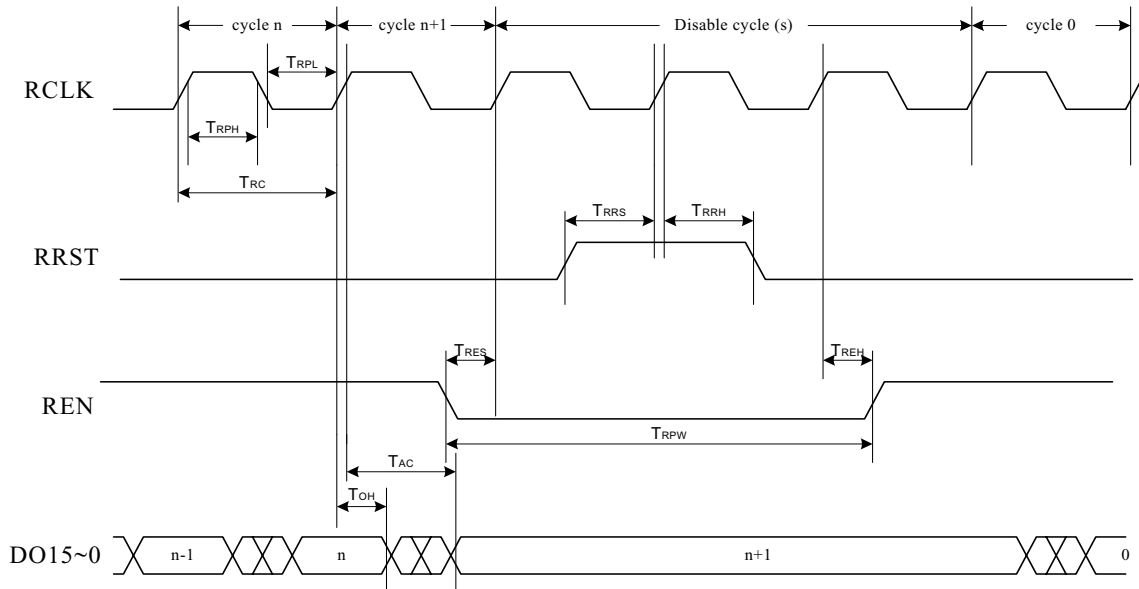
/PLRTY=GND, WEN="H", WRST="L"

Write Cycle Timing (Input Enable)



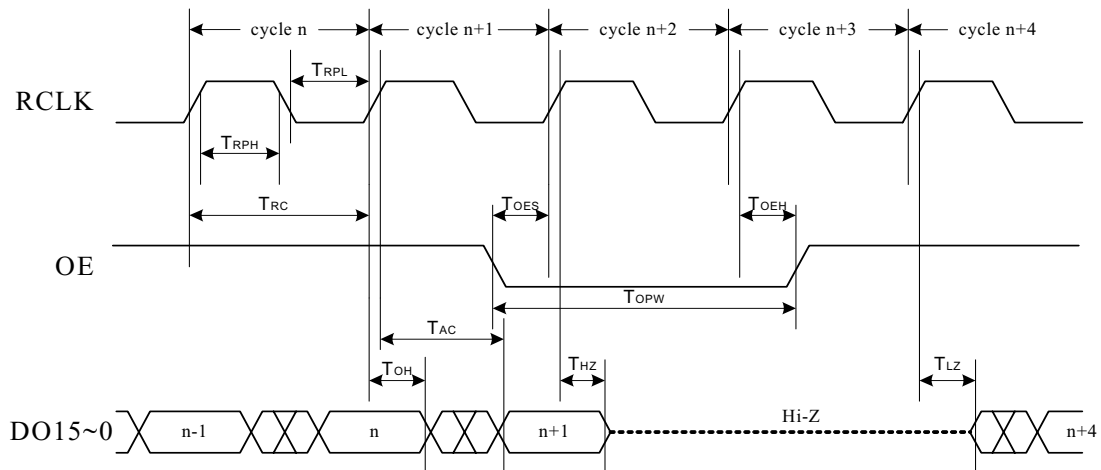
/PLRTY=GND, REN="H", OE="H"

Read Cycle Timing (Read Reset)



/PLRTY=GND, OE="H"

Read Cycle Timing (REN, RRST)



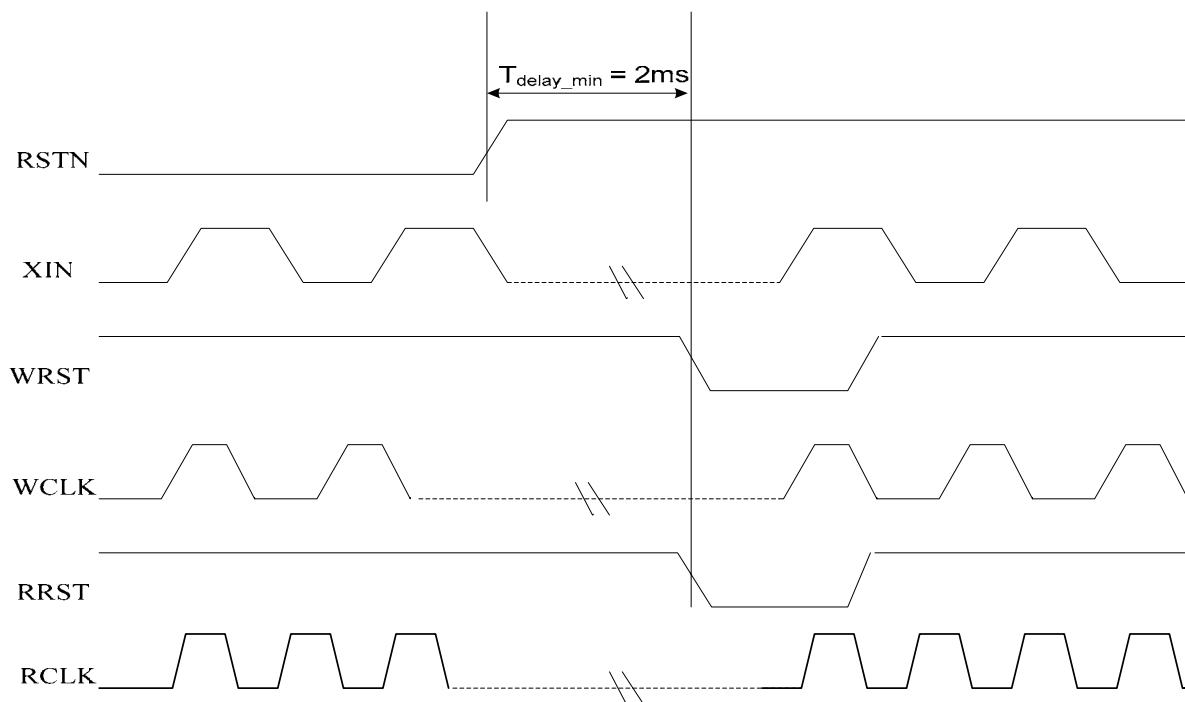
/PLRTY=GND, REN="H", RRST="L"

Read Cycle Timing (Output Enable)

8 FUNCTION DESCRIPTION

8.1 Power-On-Reset & Initialization

During system power-up, a power-on-reset is required for successful initialization of FIFO internal logic. After deactivate of its reset state, wait for $T_{\text{delay_min}}$ (2 ms) before applying any control signals to ensure the FIFO is in normal operating state. Apply a valid reset pulse of WRST and RRST after power-on-reset to guarantee Read/Write operation start at a known address (address point at zero).



/PLRTY=VDD

Chip Reset& R/W Reset Timing (Power-on-reset)

8.2 WRST, RRST Reset Operation

The reset signal can be given at any time regardless of the WEN, REN and OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again.

8.3 Control Signals Polarity Select

The AL460 provides the option for operating polarity on controlling signals. With this feature the application design can benefit by matching up the operation polarity between AL460 and an existing

interfacing devices without additional glue logic. The operating polarity of control signals WEN, REN, WRST, RRST, IE and OE are controlled by PLRTY signal. When PLRTY is pulled high all 6 signals will be active low. When PLRTY is pulled low all 6 signals will be active high.

8.4 FIFO Write Operation

In the FIFO write operation, 16 bits of write data are input in synchronization with the WCLK clock. The FIFO write operation is determined by WRST, WEN, IE and WCLK signals and the combination of these signals could produce different write result. The PLRTY signal determines the activated polarity of these control signals. The following tables describe the WRITE functions under different operating polarities.

PLRTY = VDD

WRST	WEN	IE	WCLK	Function
L	-	-	↑	Write reset. The write pointer is reset to zero.
H	L	L	↑	Normal Write operation.
H	L	H	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
H	H	-	↑	Write operation stopped. Write address pointer is also stopped.

PLRTY = GND

WRST	WEN	IE	WCLK	Function
H	-	-	↑	Write reset. The write pointer is reset to zero.
L	H	H	↑	Normal Write operation.
L	H	L	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
L	L	-	↑	Write operation stopped. Write address pointer is also stopped.

8.5 FIFO Read Operation

In the FIFO read operation, 16 bits of read data are available in synchronization with the RCLK clock. The access time is stipulated from the rising edge of the RCLK clock. To ensure valid data read, minimum of 1.5 Kbyte data write has to occur before any read operations. The FIFO read operation is determined by RRST, REN, OE and RCLK signals, the combination of these signals could produce varying read results. The PLRTY signal could decide the activated polarity of these control signals. The following tables describe the READ functions under different operating polarities.

PLRITY = VDD

RRST	REN	OE	RCLK	Function
L	L	L	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
L	L	H	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
L	H	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.
L	H	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
H	L	L	↑	Normal Read operation.
H	L	H	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
H	H	L	↑	Read address pointer is stopped. Output data is held.
H	H	H	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

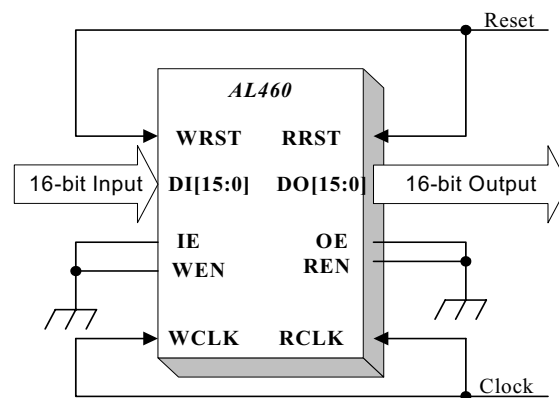
PLRITY = GND

RRST	REN	OE	RCLK	Function
H	H	H	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
H	H	L	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
H	L	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after REN goes low.
H	L	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after REN goes low.
L	H	H	↑	Normal Read operation.
L	H	L	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
L	L	H	↑	Read address pointer is stopped. Output data is held.
L	L	L	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

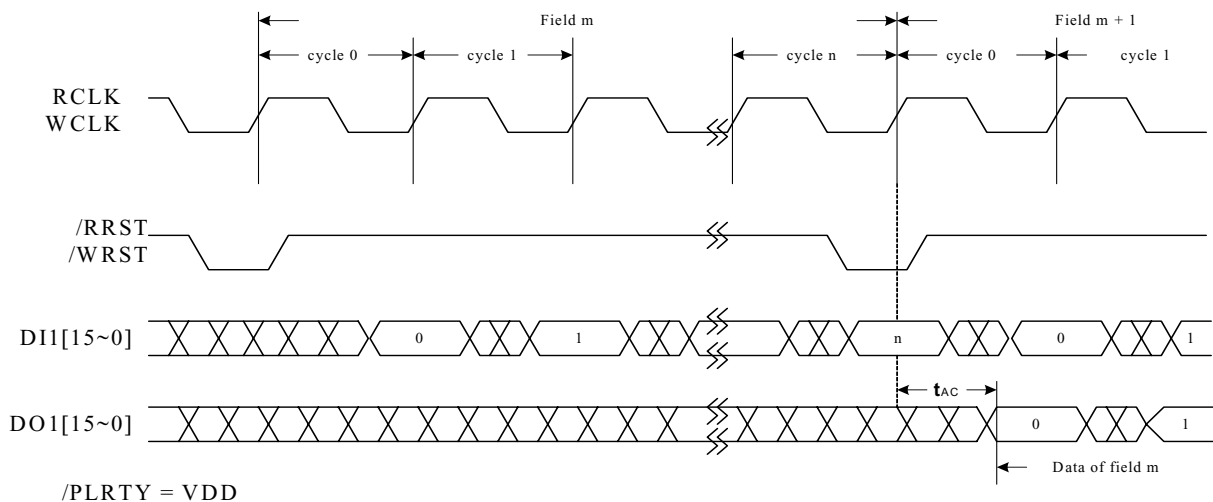
9 APPLICATION NOTE

9.1 One Field Delay Line (The Old Data Read)

As the design shown in the diagram by applying the reset every 1-field cycle (with the common signal for WRST and RRST) and a constant read/write operation (with all WEN, REN, IE and OE are tied to active status), "1 field delay line" timing is shown in timing chart below. When the difference between the write address and the read address is 0 (the read address and the write address are the same), the old field data are read as shown in the timing chart.



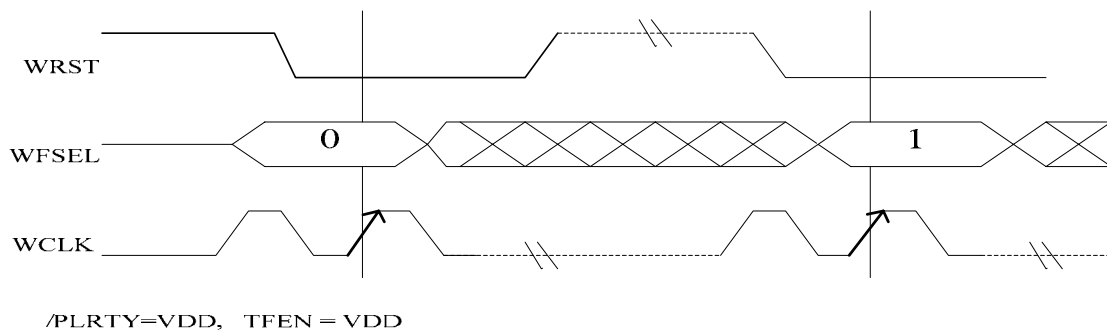
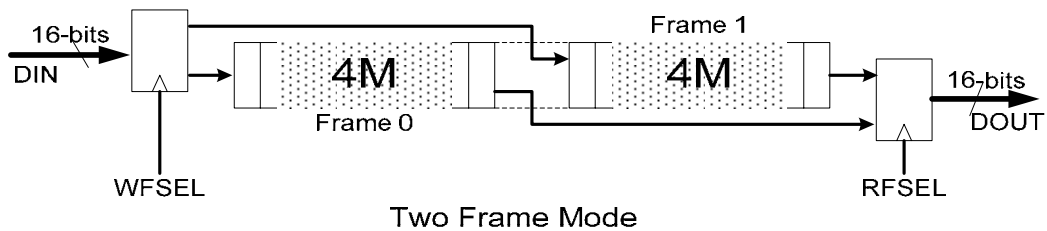
AL460 1 Field Delay Line Diagram



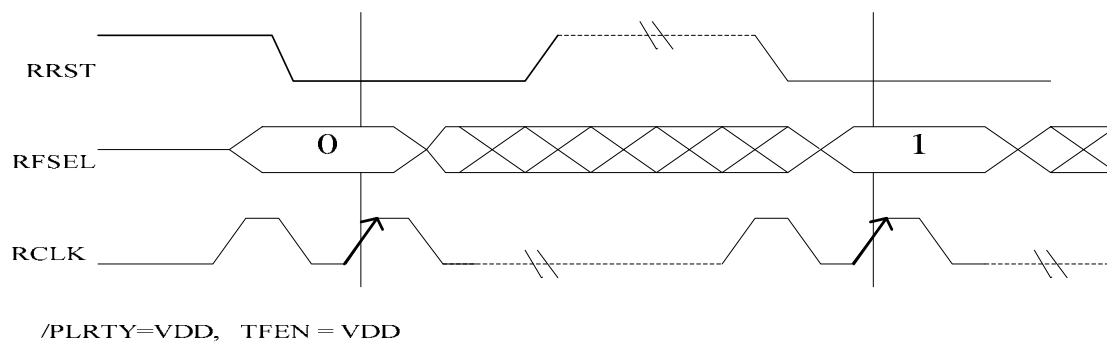
AL460 1 Field Delay Line Timing Diagram

9.2 Two Frame Mode

Two Frame buffering mechanism enables AL460 to store two complete frames simultaneously. This advantage makes it possible to process two separated frames in parallel for enhancing performance. Read/Write of a desired frame is allocated via R/W frame select pins. The R/W frame selection and control manipulation are illustrated in the following diagrams.



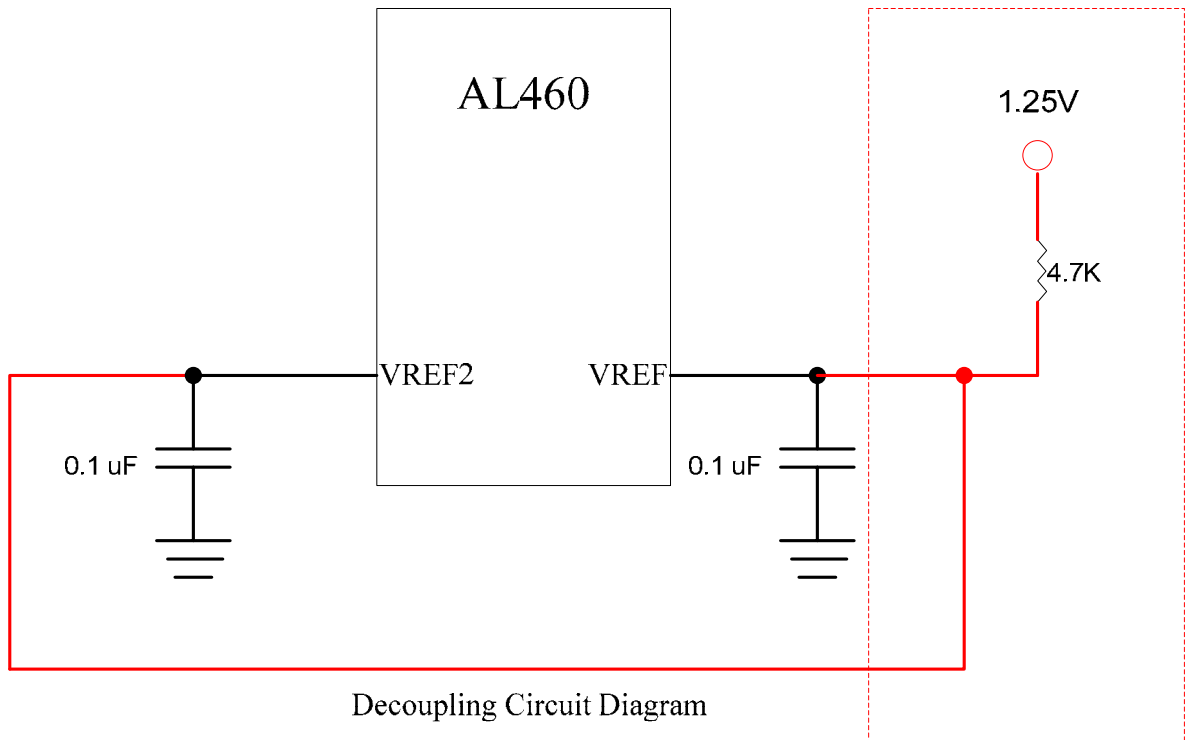
Write Frame Select (WFSEL) Timing Diagram



Read Frame Select (RFSEL) Timing Diagram

9.3 External Decoupling Circuit

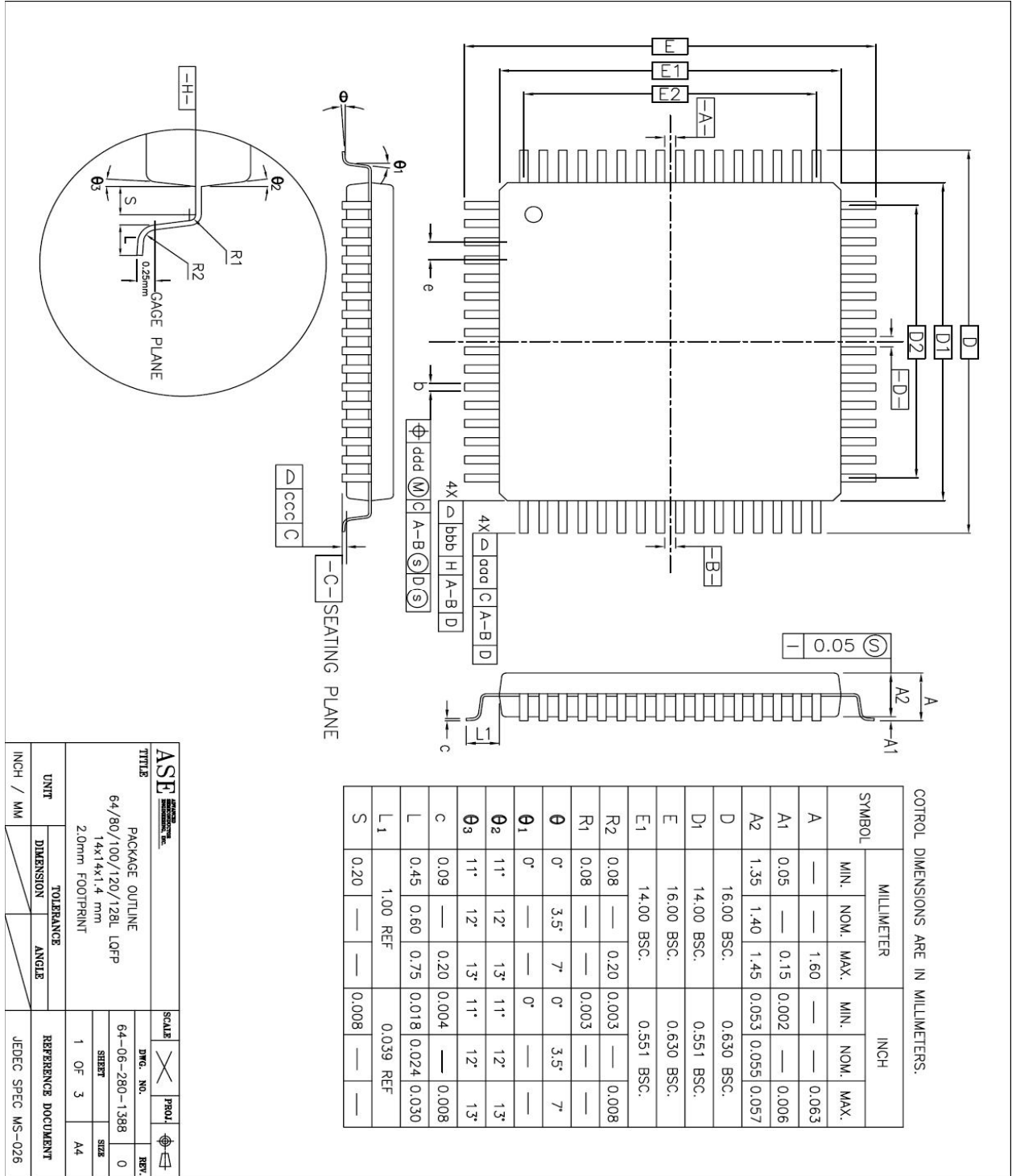
To ensure the proper operation of internal memory, an external decoupling circuit must be implemented.



Note: The 1.25V reference input voltage circuit (Red) is optional

10 Mechanical Drawing – 128 PIN LQFP

10.1 14x14x1.4mm 128-Pin LQFP Package



ASE <small>Advanced Semiconductor Engineering, Inc.</small>		SCALE	PROJ.	REV.
TITLE PACKAGE OUTLINE 64/80/100/120/128L LQFP 14x14x1.4 mm 2.0mm FOOTPRINT		DWG. NO.	64-06-280-1388	0
UNIT INCH / MM		SHEET	1 OF 3	SIZE A4
DIMENSION TOLERANCE ANGLE		REFERENCE DOCUMENT JEDEC SPEC MS-026		

SYMBOL	64L			80L			100L			120L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.22	0.30	0.38	0.009	0.012	0.015
e	0.80	BSC.		0.031	BSC.		0.65	BSC.		0.026	BSC.	
D2	12.00			0.472			12.35			0.486		
E2	12.00			0.472			12.35			0.486		
ggg	0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008		
ccc	0.10			0.004			0.10			0.004		
ddd	0.20			0.008			0.13			0.005		

TOLERANCES OF FORM AND POSITION

SYMBOL	128L		
	MIN.	NOM.	MAX.
b	0.13	0.16	0.23
e	0.40	BSC.	0.016 BSC.
D2	12.40		0.488
E2	12.40		0.488
ggg	0.20		0.008
bbb	0.20		0.008
ccc	0.08		0.003
ddd	0.07		0.003

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
- ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

ASE ADVANCED SEMICONDUCTOR ENGINEERING		SCALE	<input checked="" type="checkbox"/> DWG. NO.	PROJ.	<input checked="" type="checkbox"/>	REV.	<input type="checkbox"/>
TITLE		PACKAGE OUTLINE		64-06-280-1388		0	
64/80/100/120/128L LOFP		14x14x1.4 mm		2 OF 3		A4	
UNIT		TOLERANCE		REFERENCE DOCUMENT		JEDEC SPEC MS-026	
INCH / MM		DIMENSION		ANGLE			
		2.0mm FOOTPRINT					

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